

FIG. 1

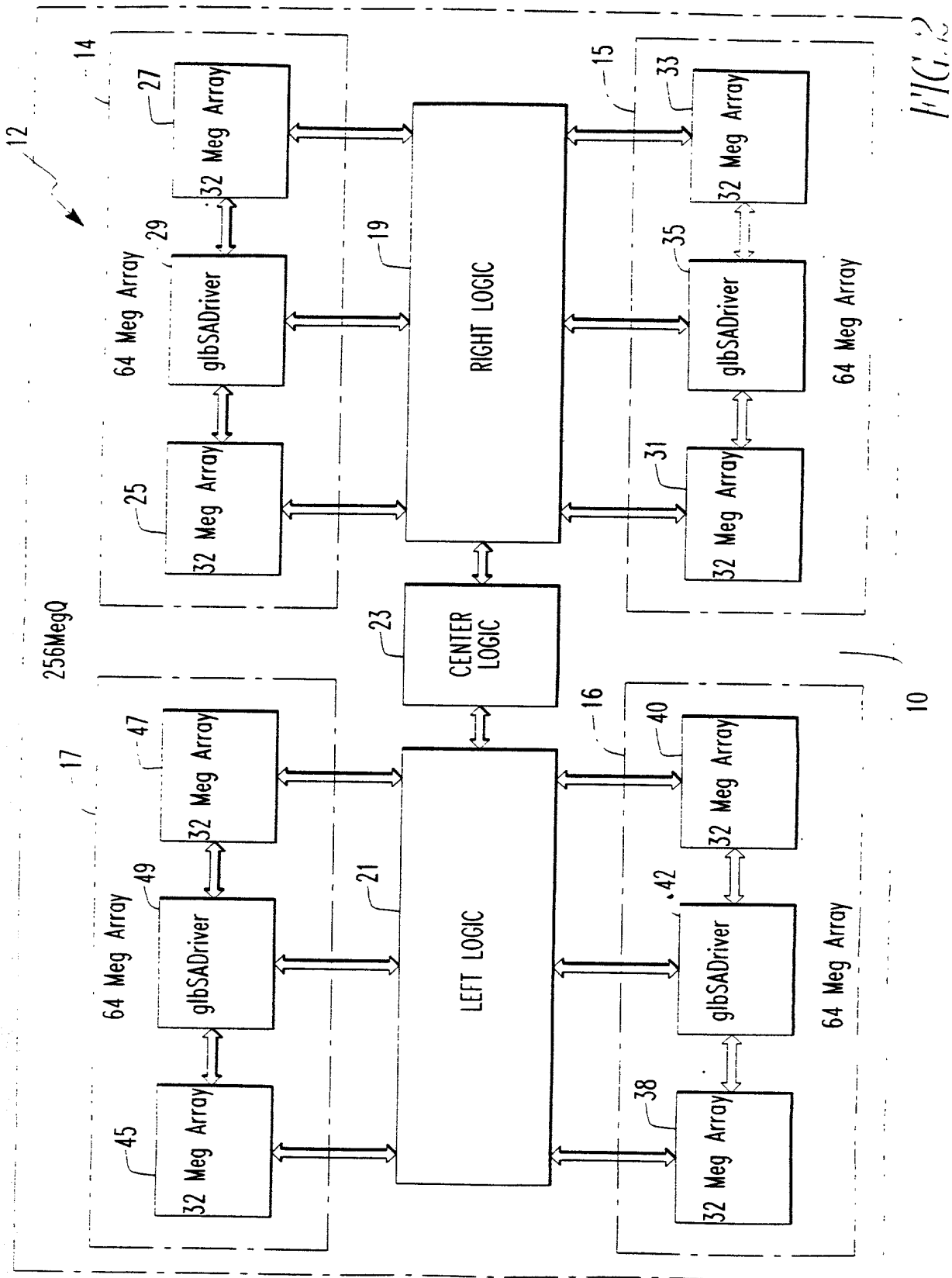


FIG. 3A

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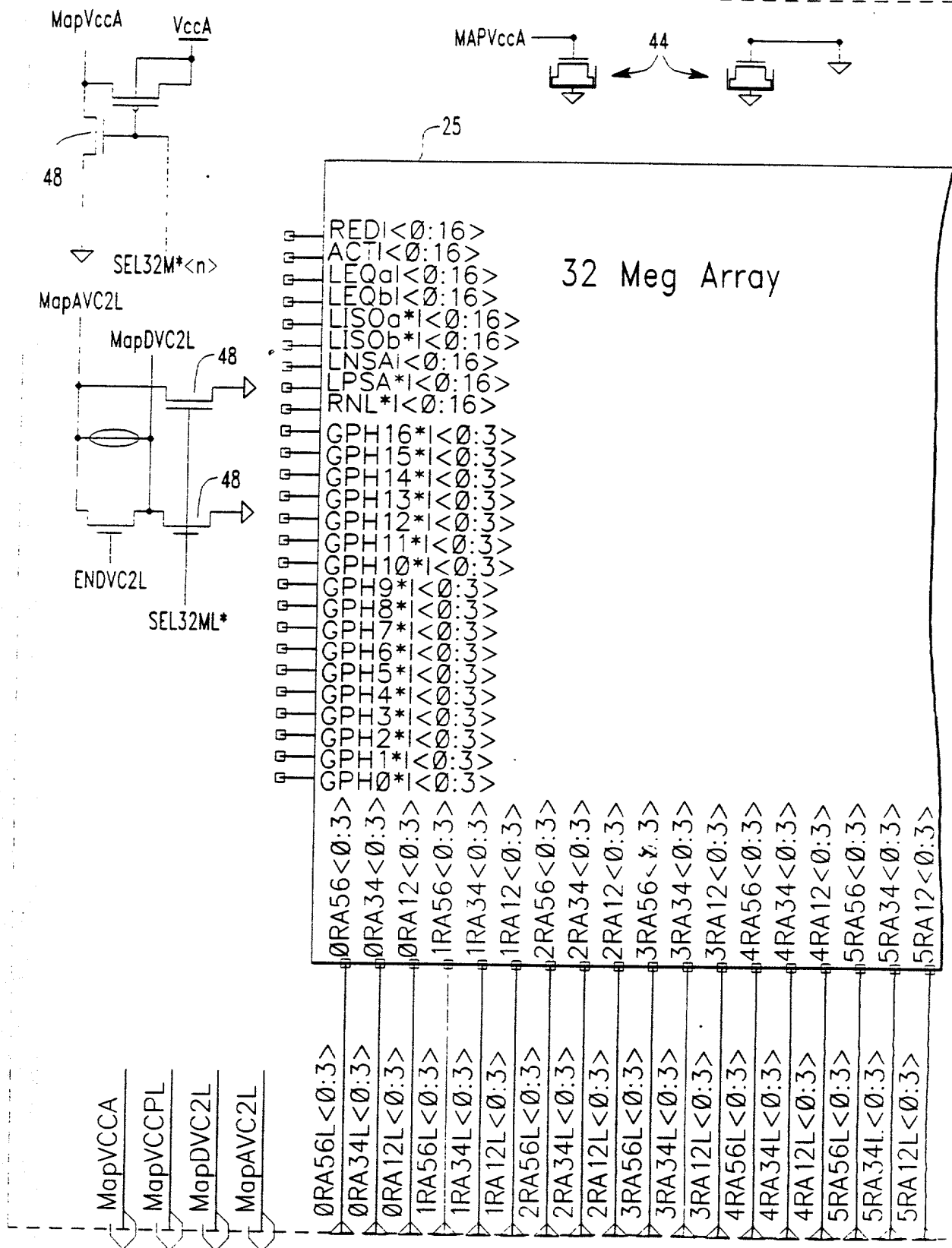
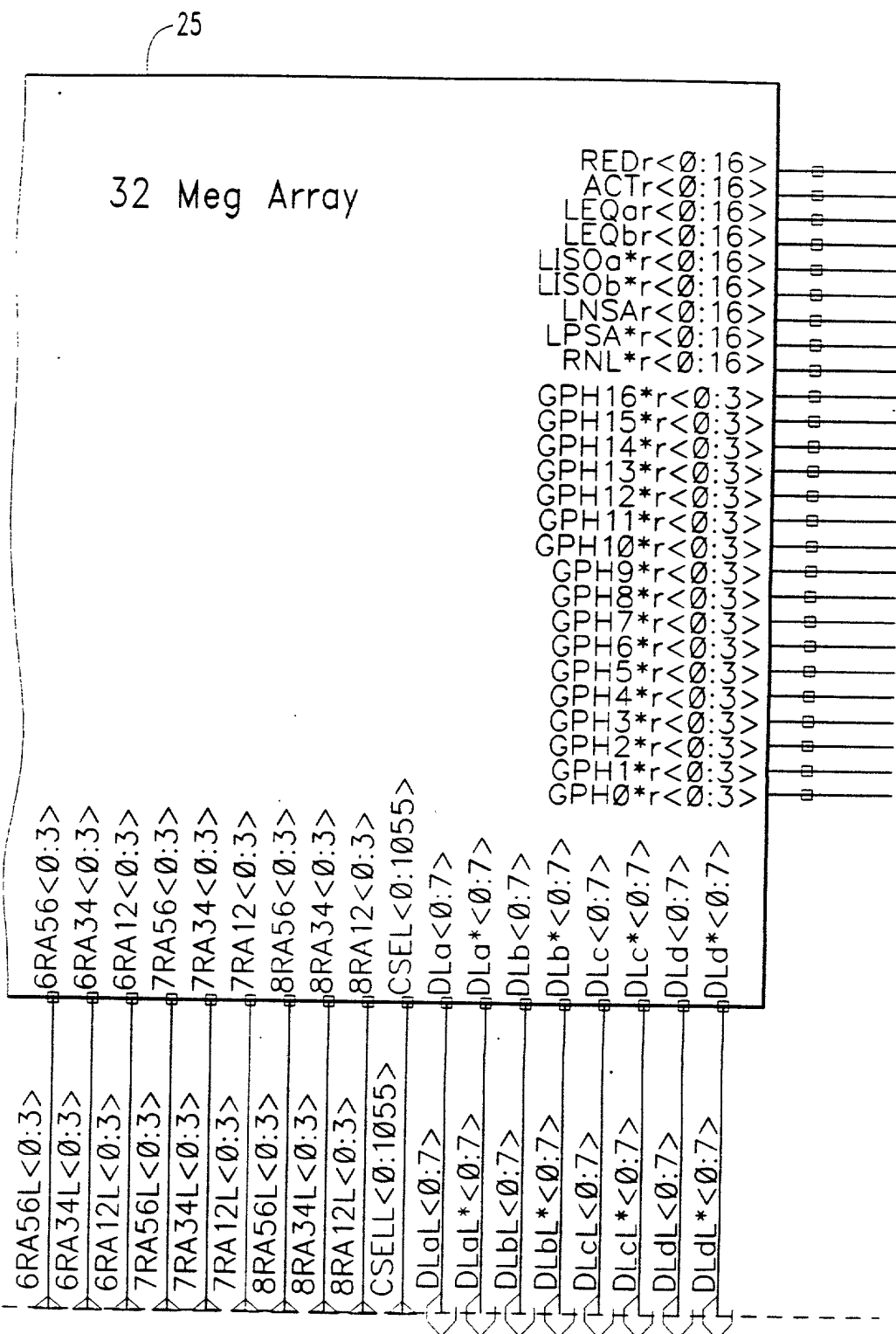


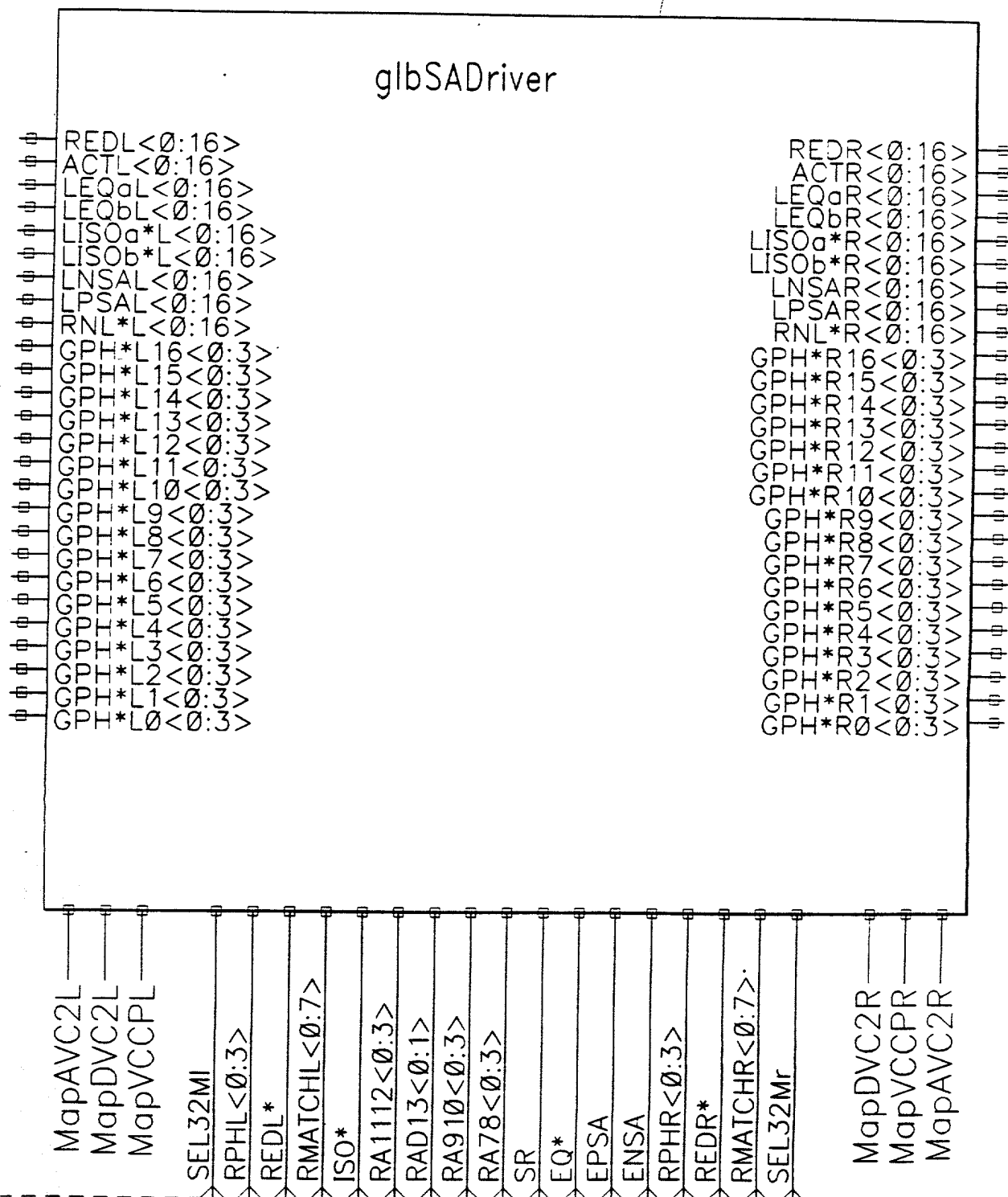
FIG. 3B

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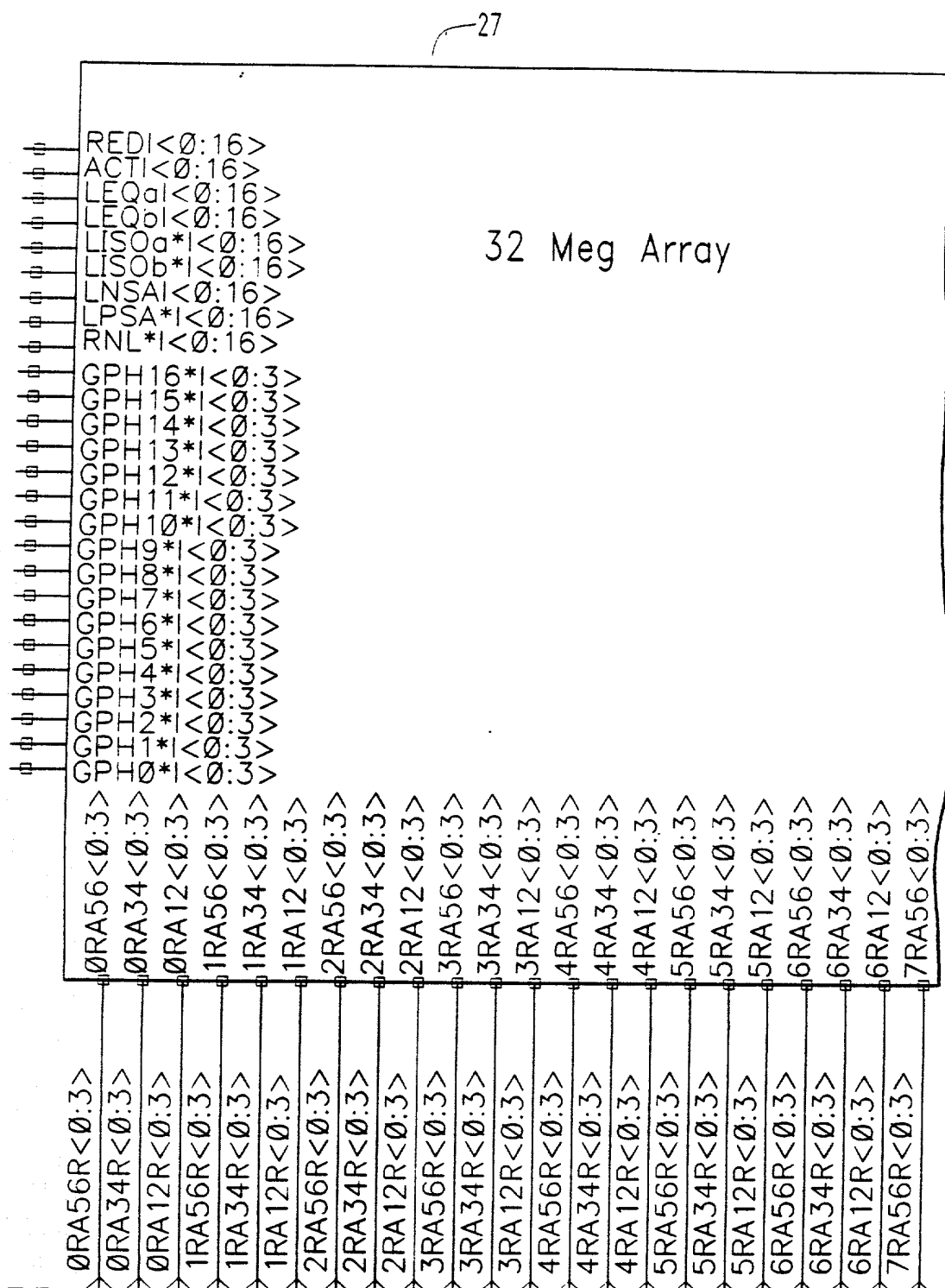


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## 32MEG ARRAY

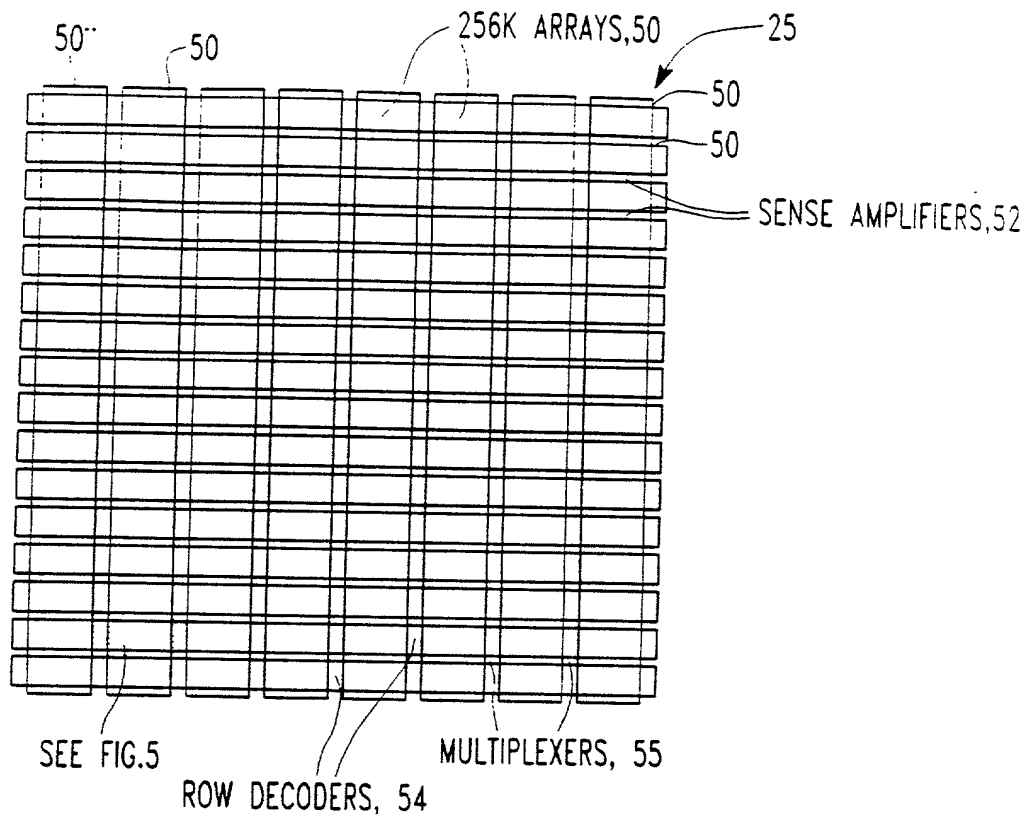


FIG. 4



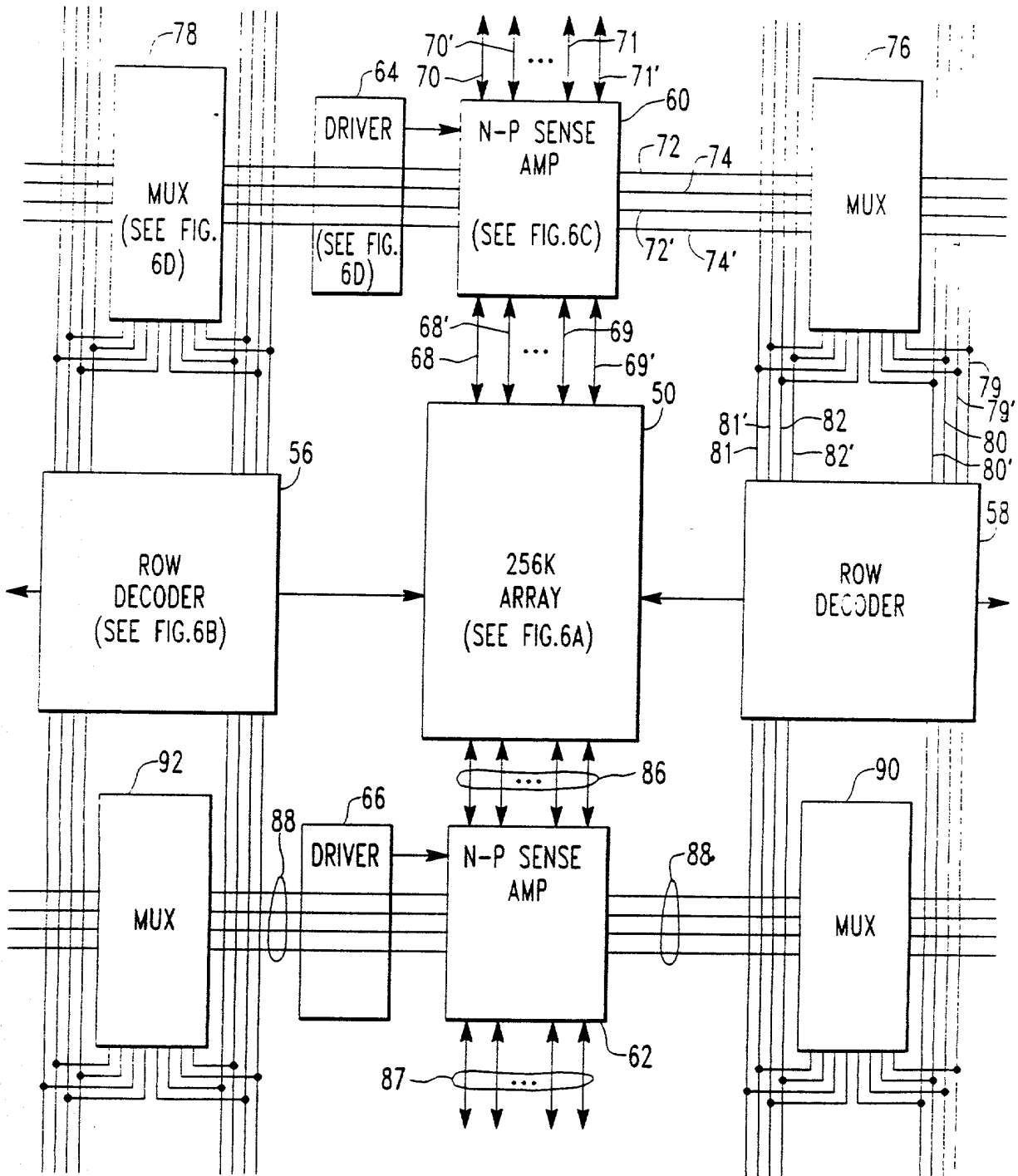


FIG. 5

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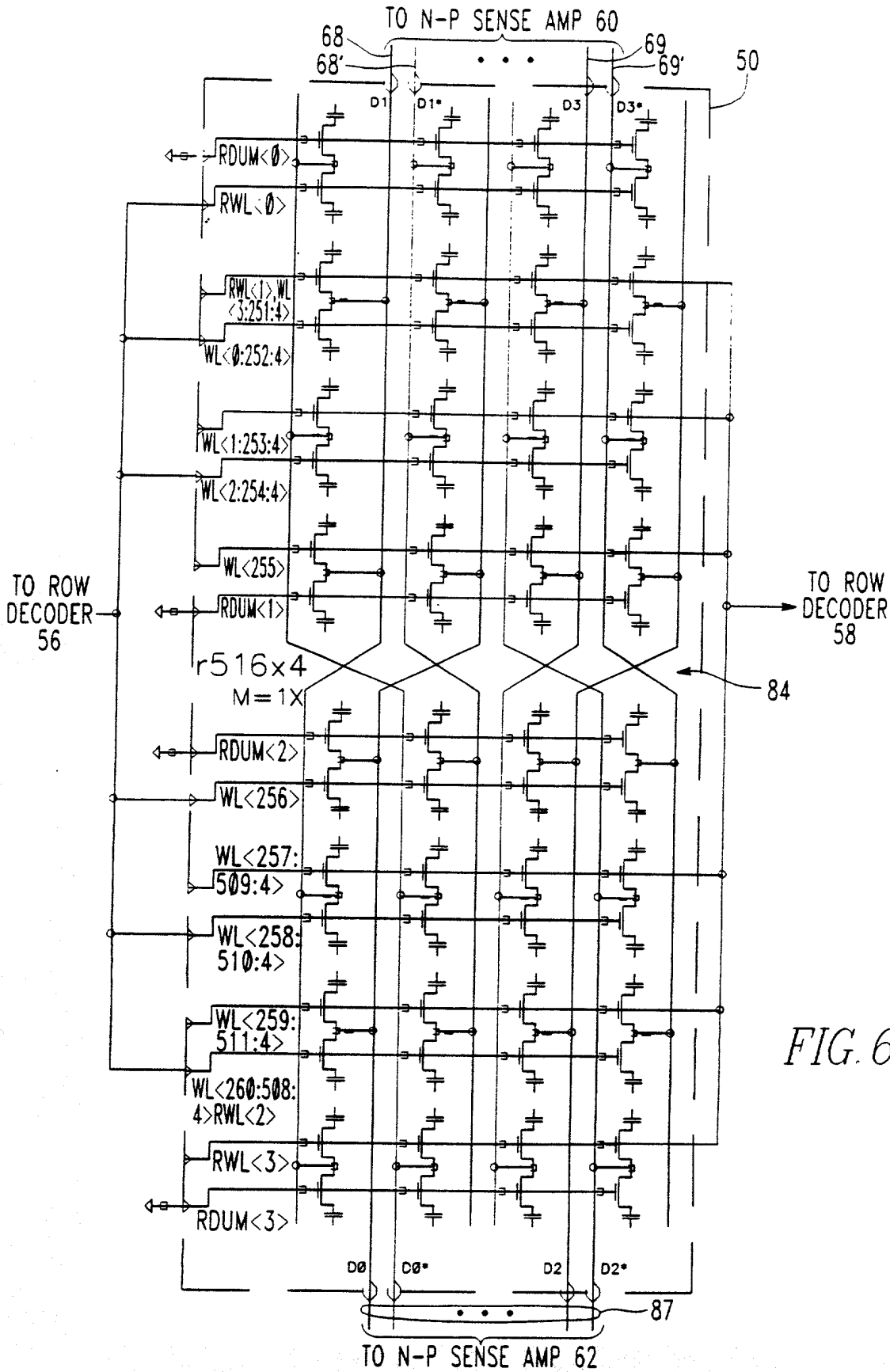


FIG. 6A

DATA LINES

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DATA LINES

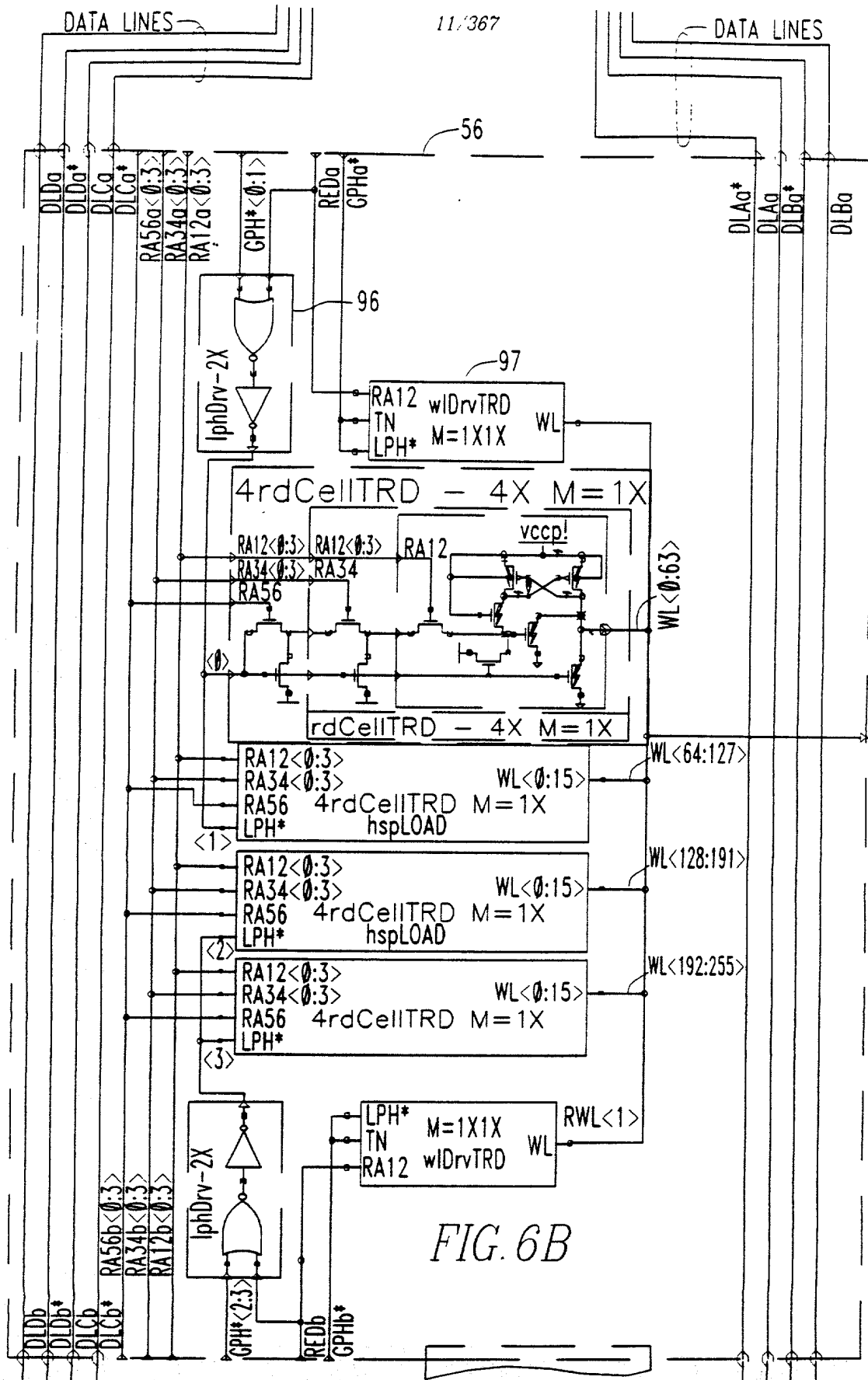


FIG. 6B

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Connections of odd/even  
columns to IOa and IOb  
alternates with odd/even  
column select lines:  
CA01\* D1(even) D2(odd)

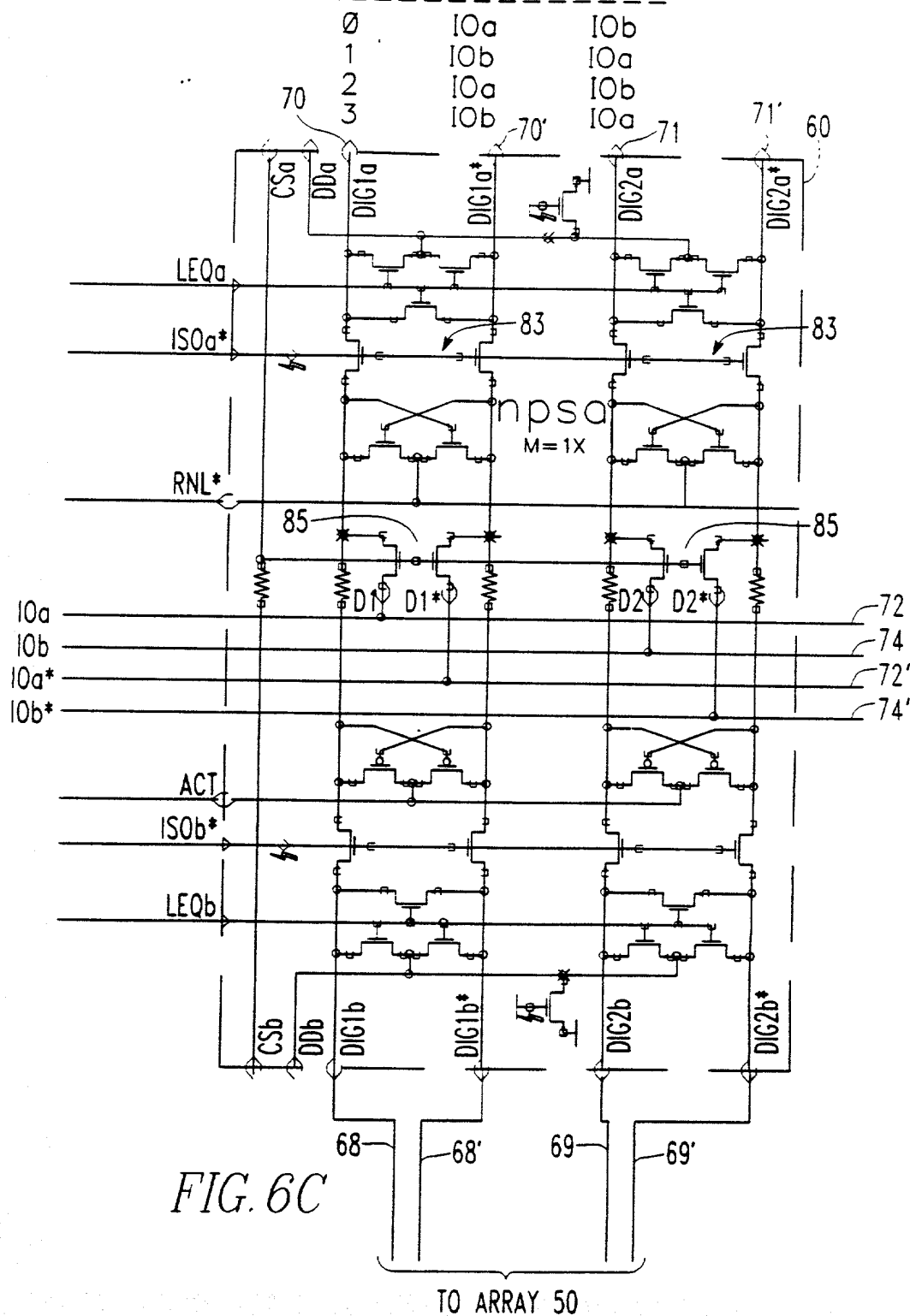


FIG. 6C

TO ARRAY 50

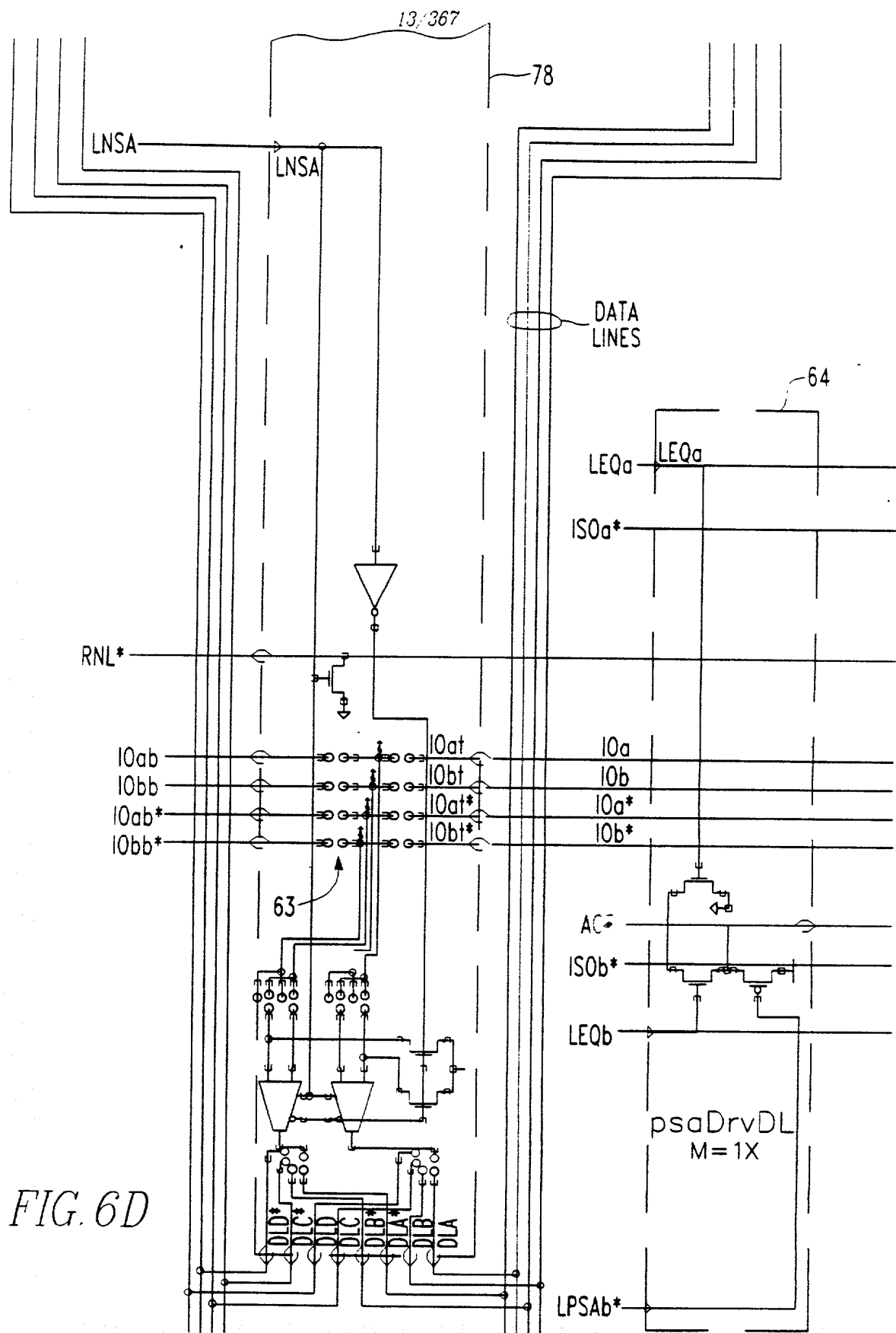
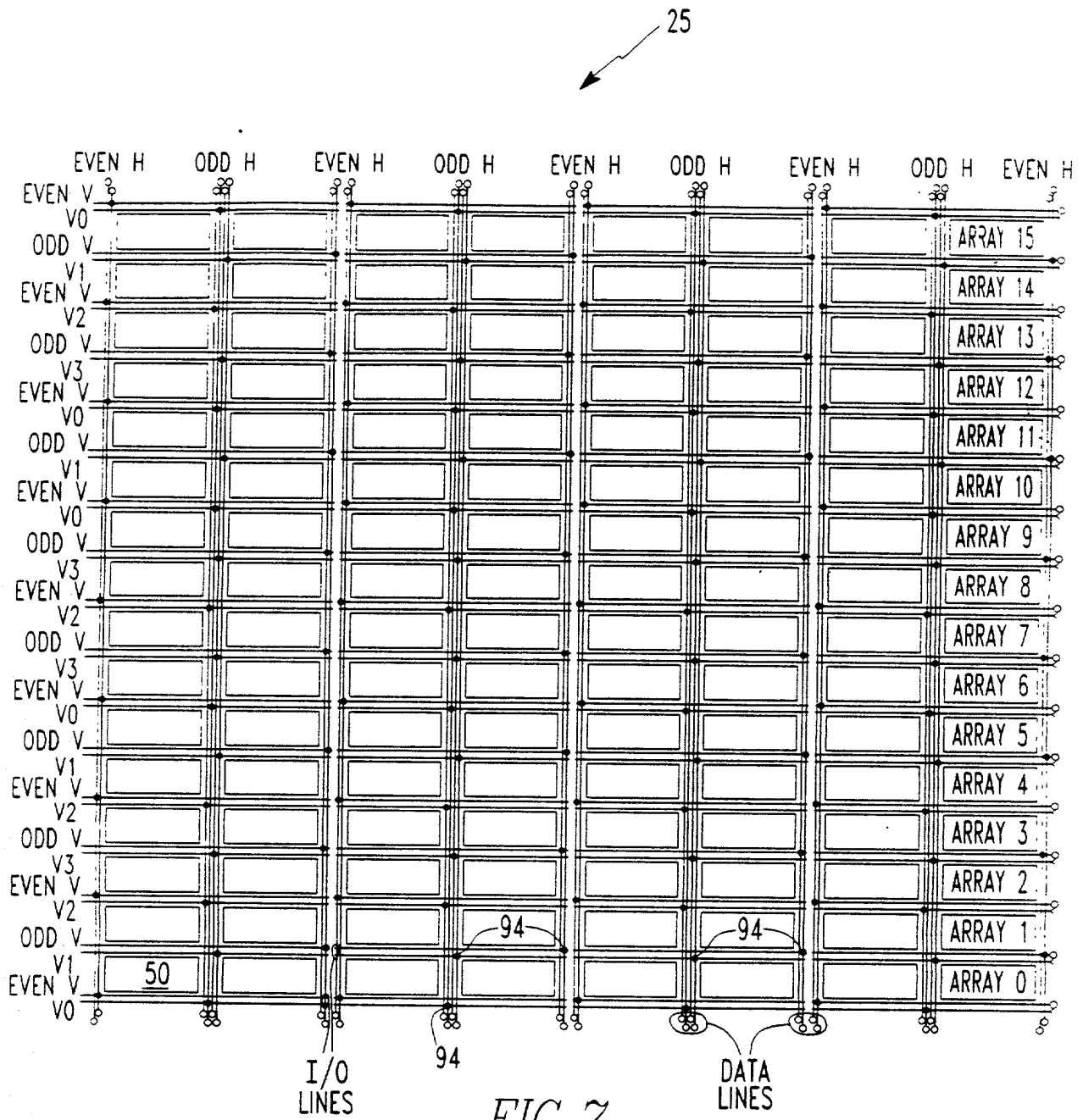


FIG. 6D



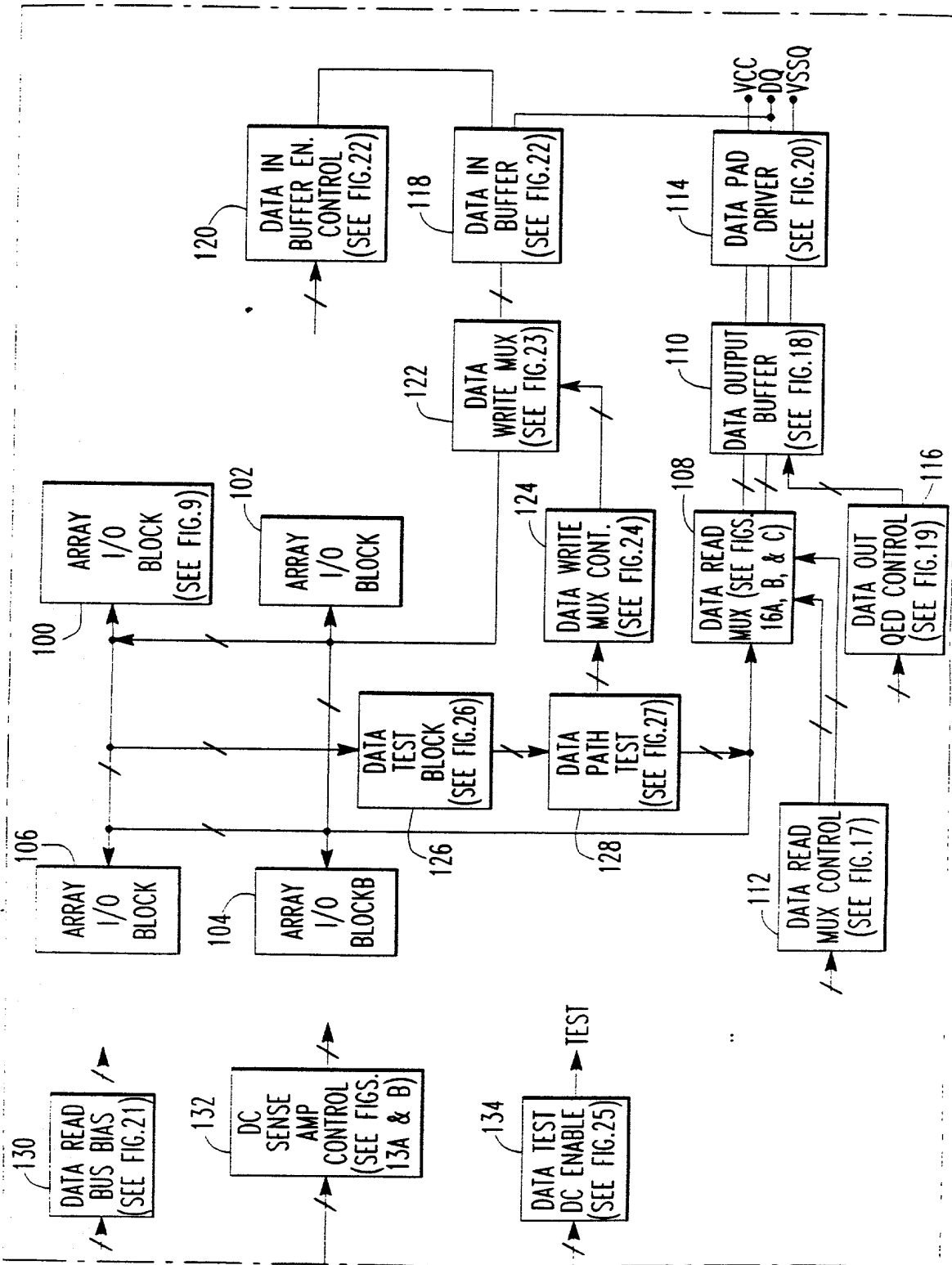


FIG. 8

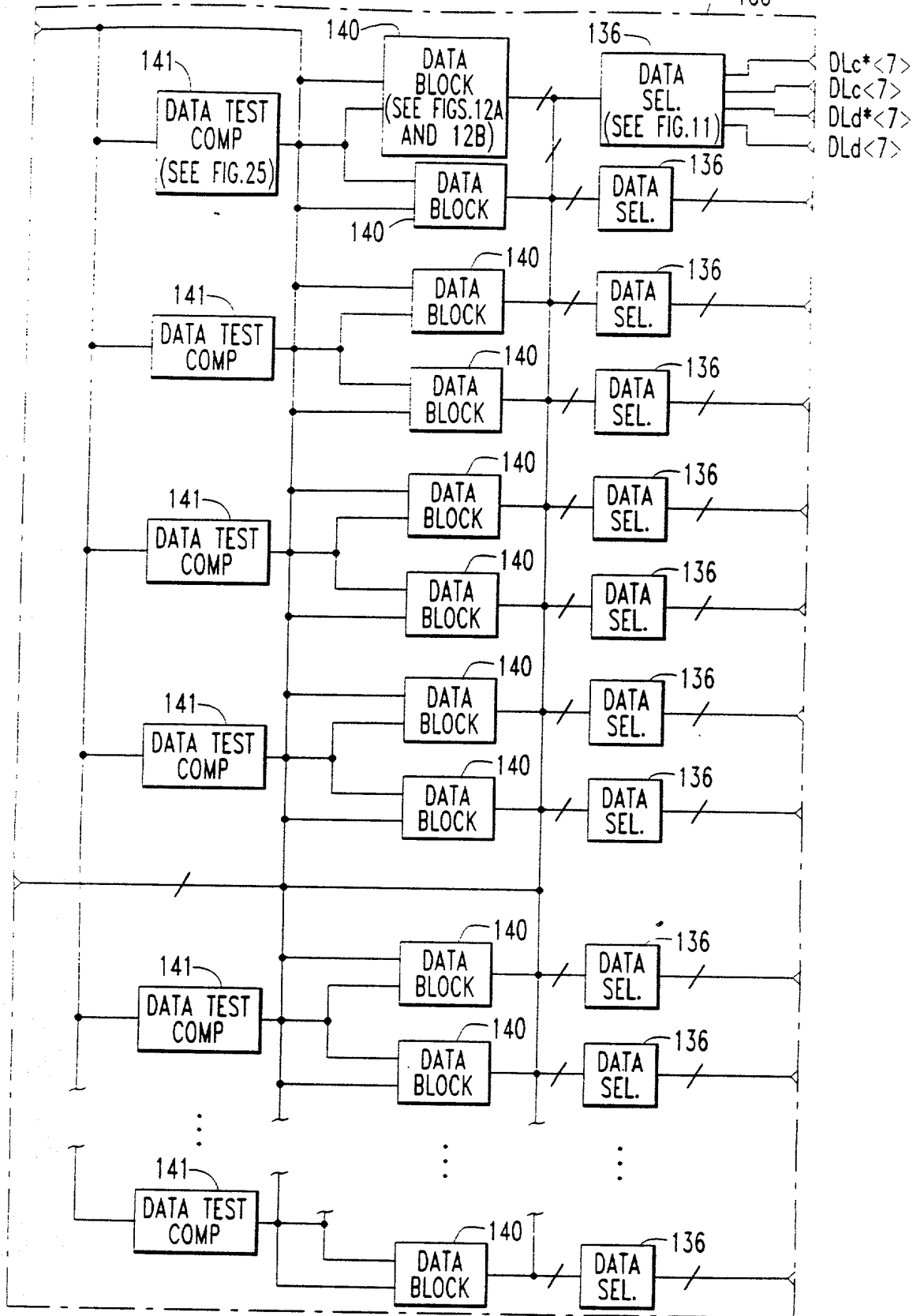


FIG. 9



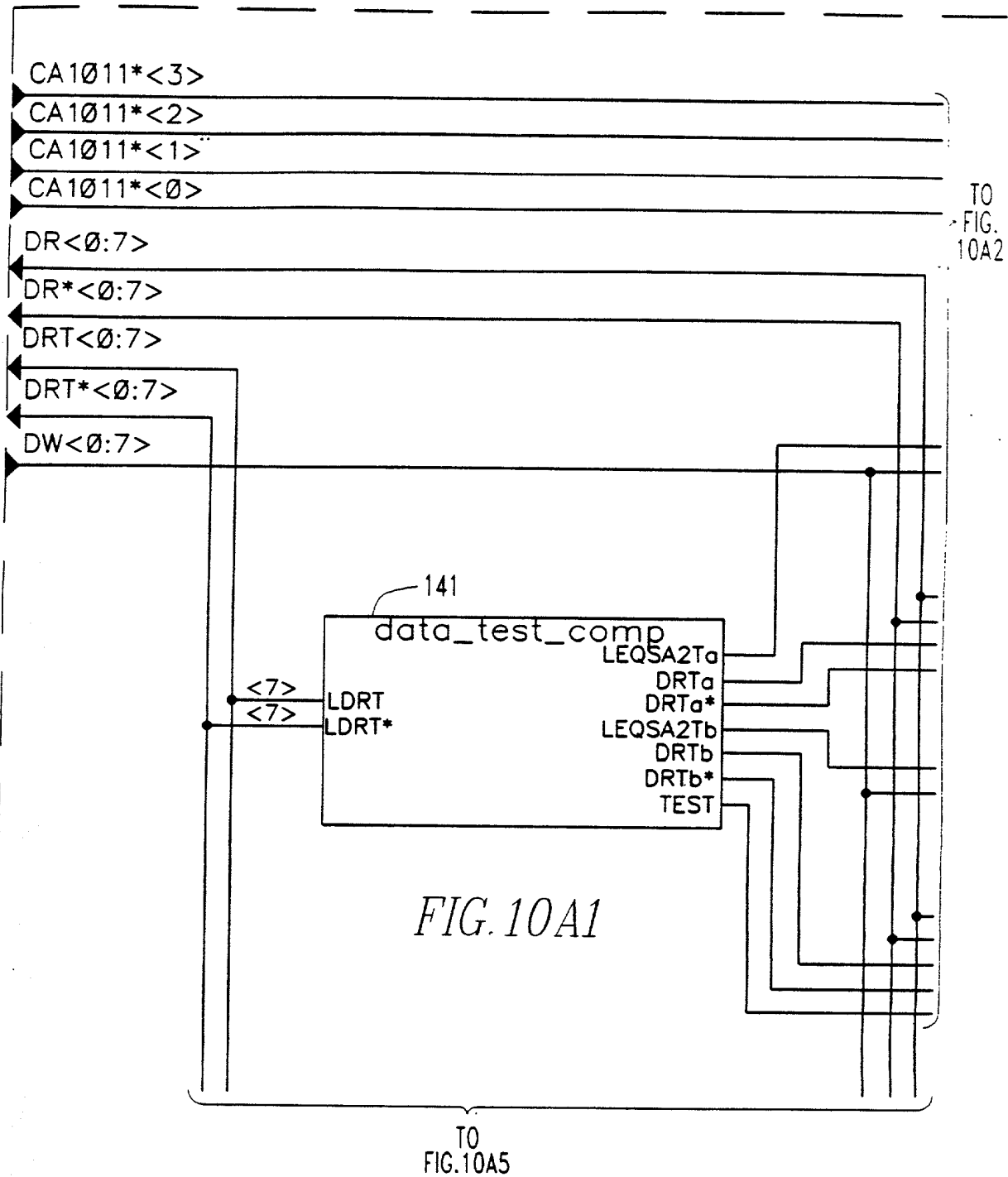


FIG. 10A2

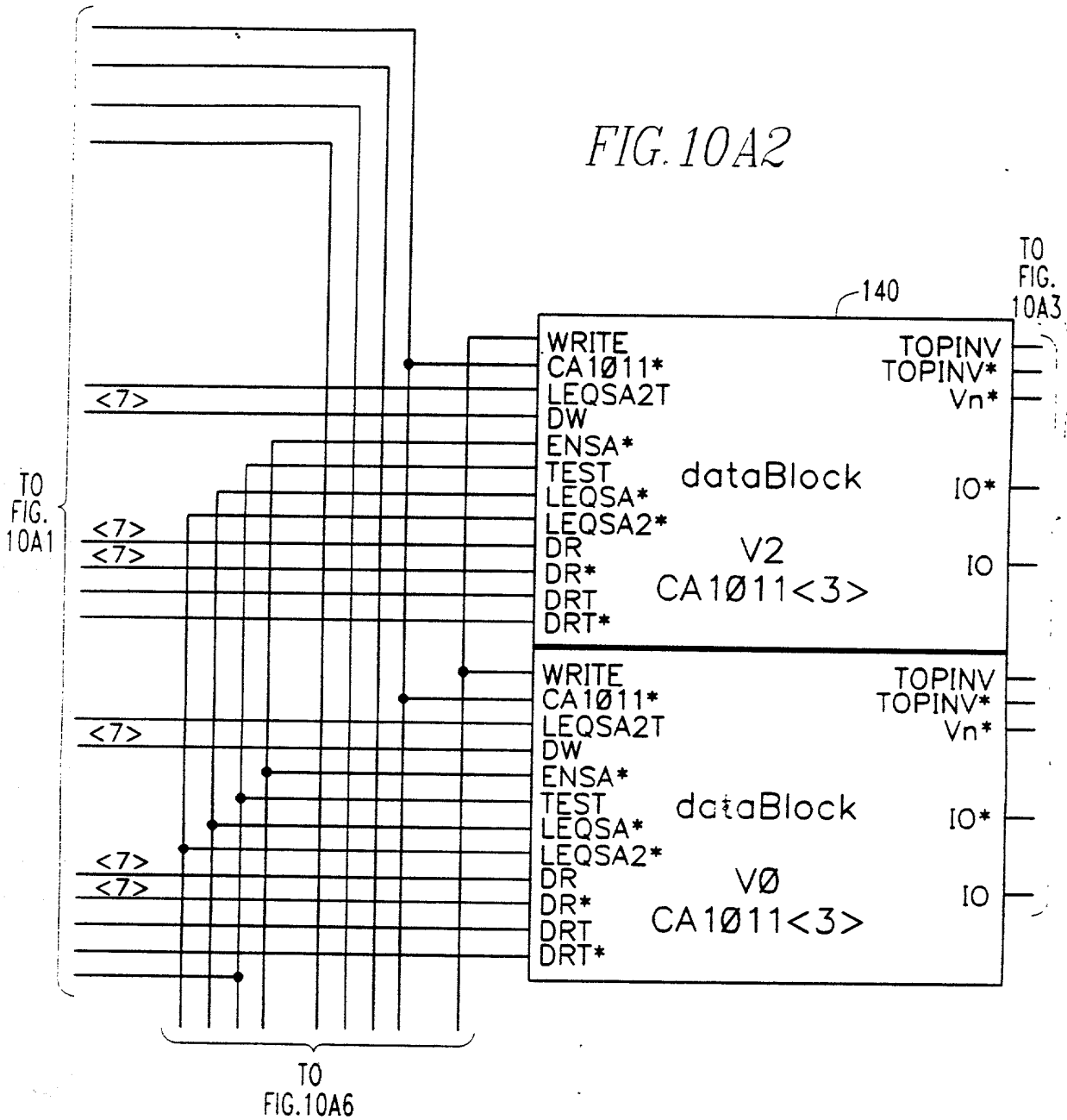
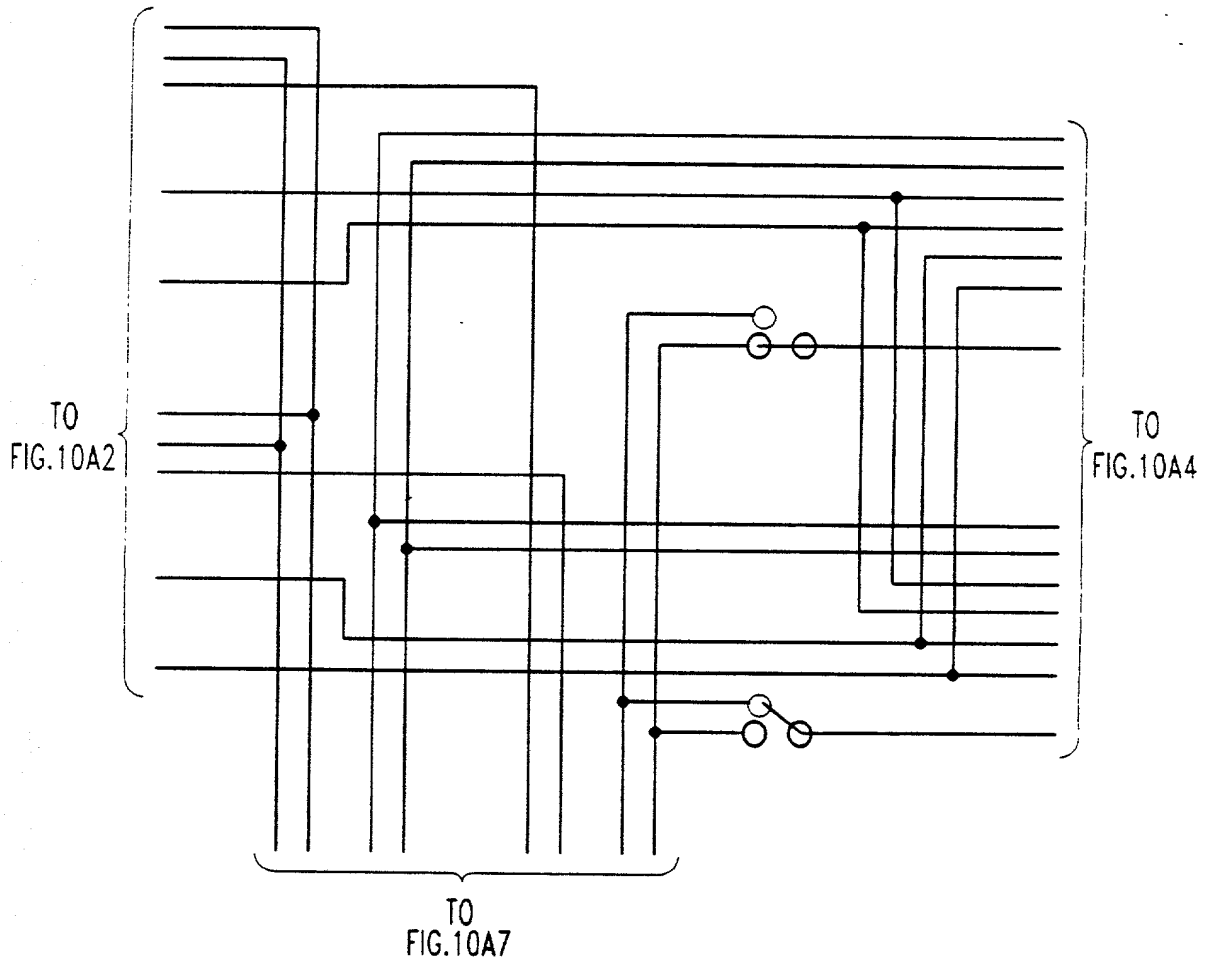


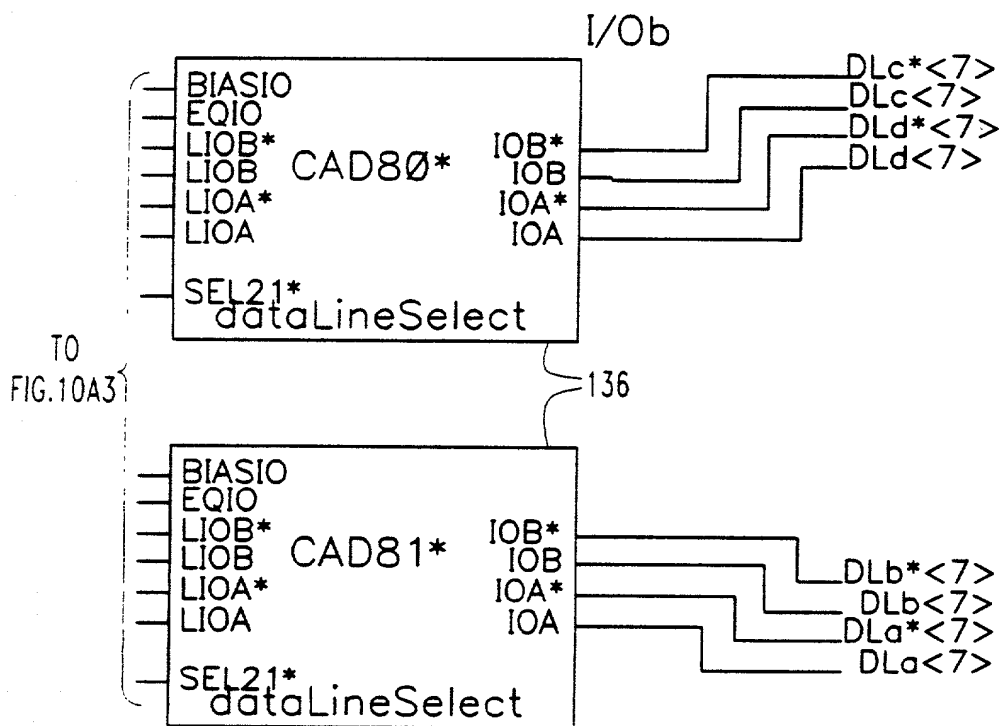
FIG. 10A3



arrayIOBlock

100

FIG. 10A4



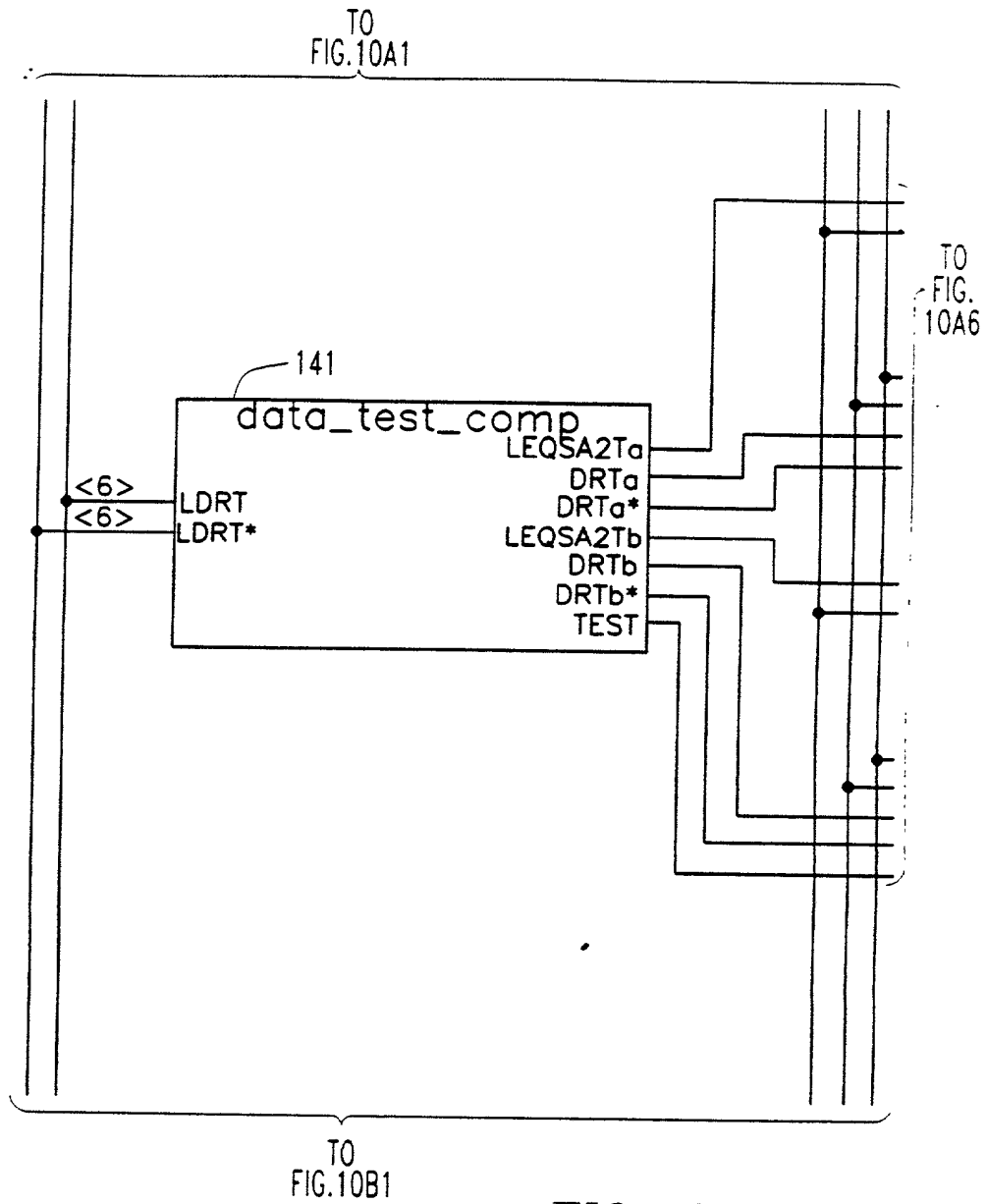


FIG. 10A5

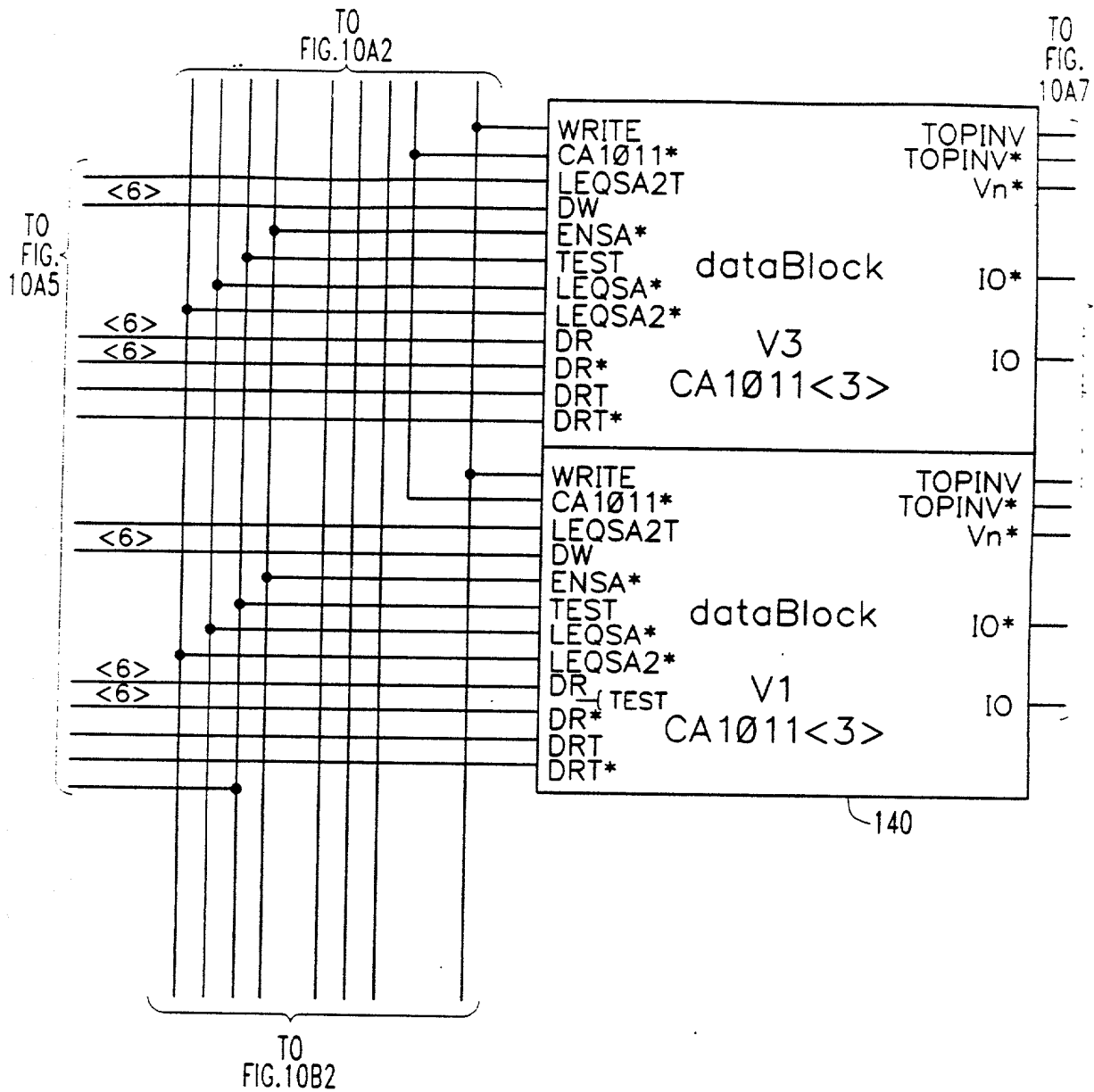


FIG. 10A6

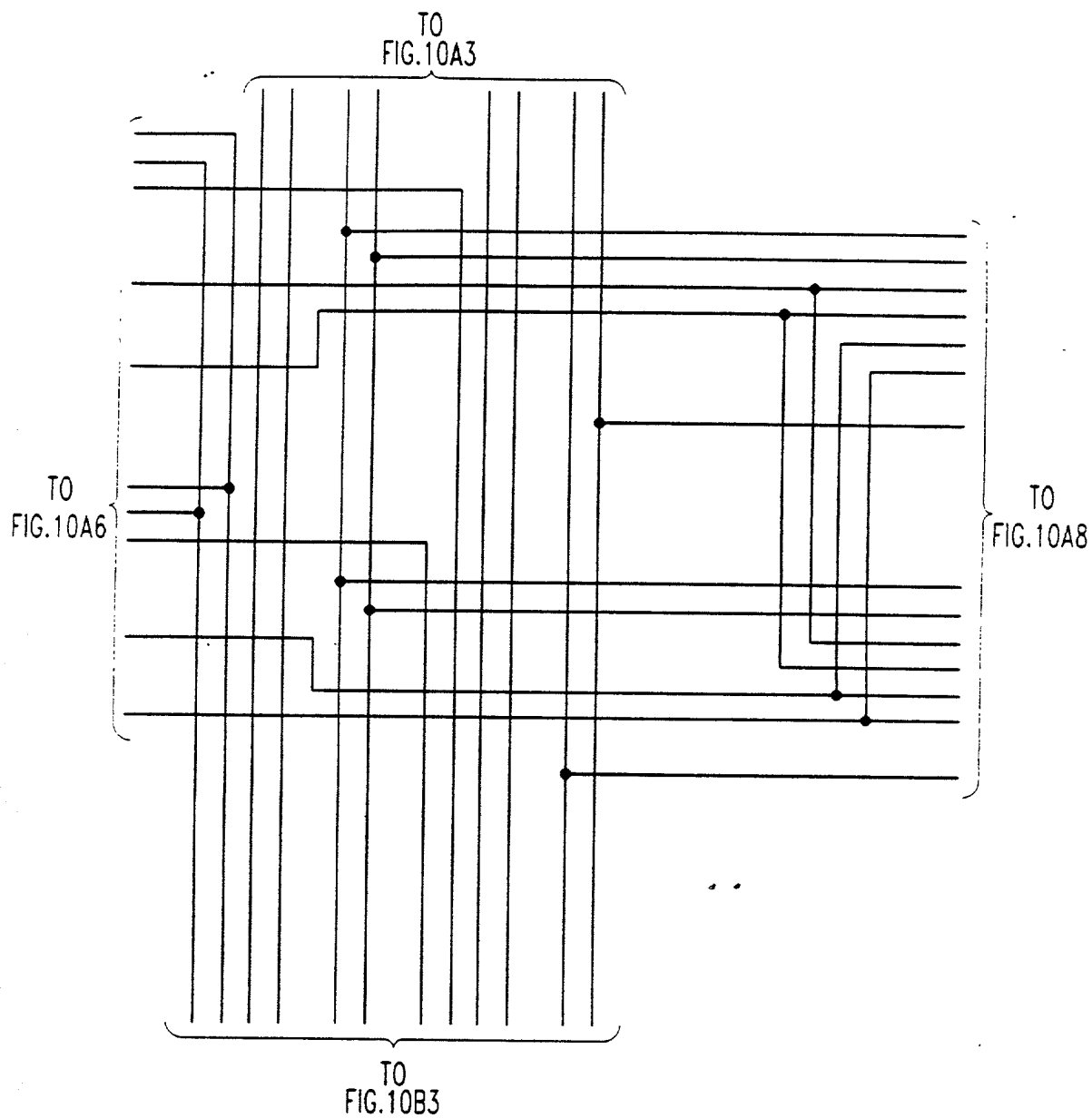


FIG. 10A7

I/Oa

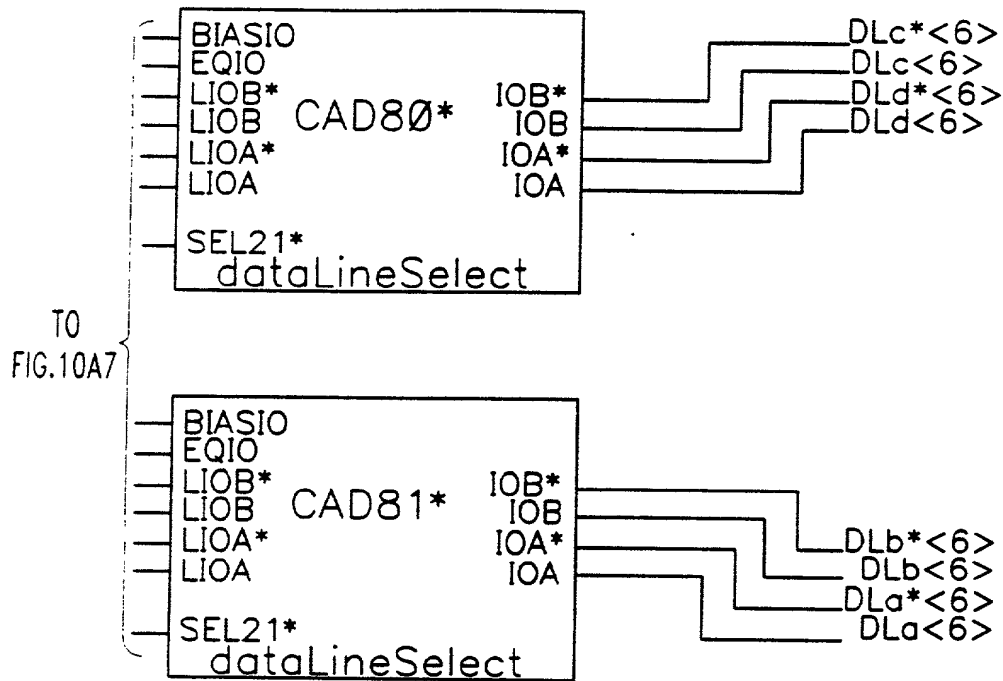


FIG.10A8



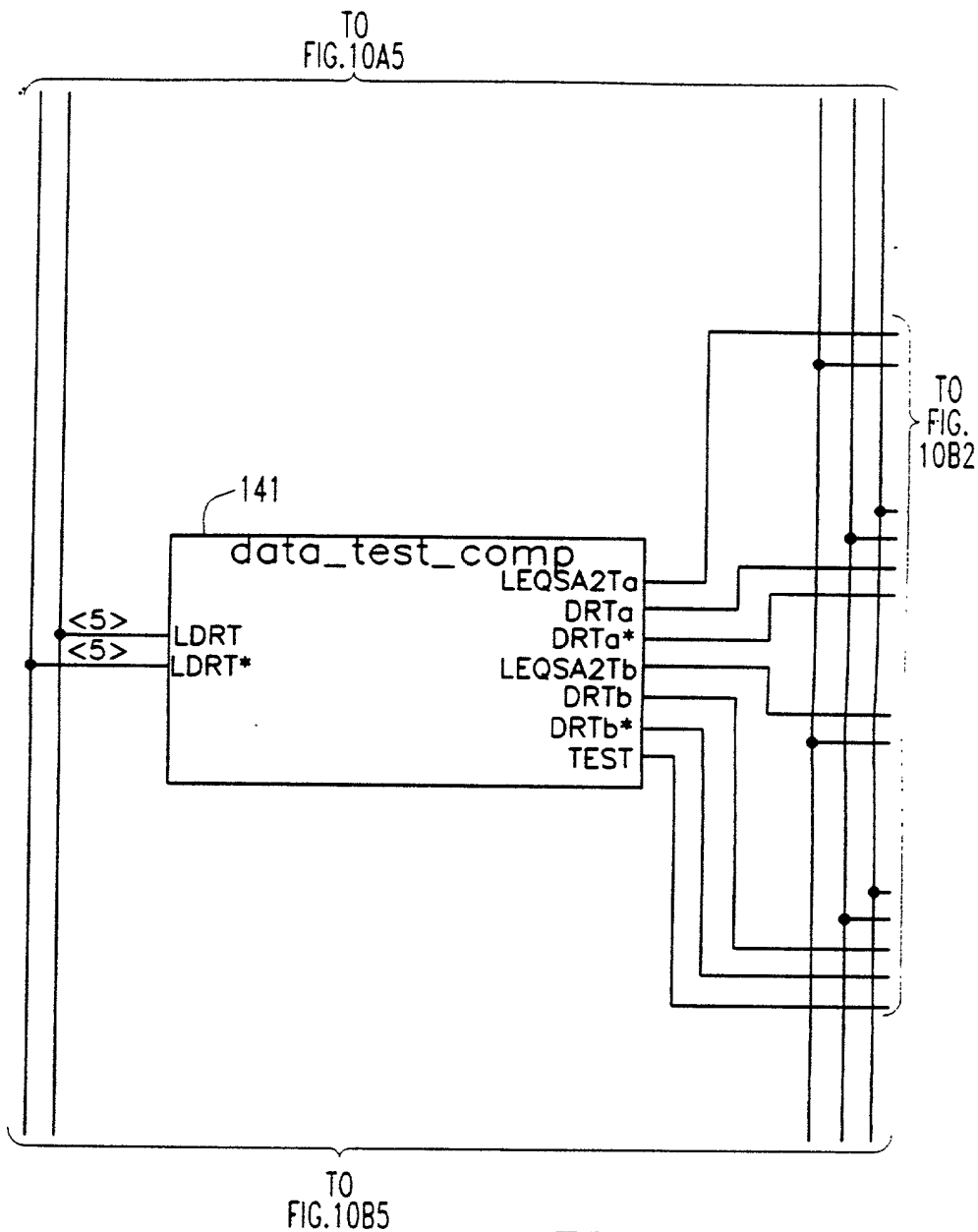


FIG. 10B1

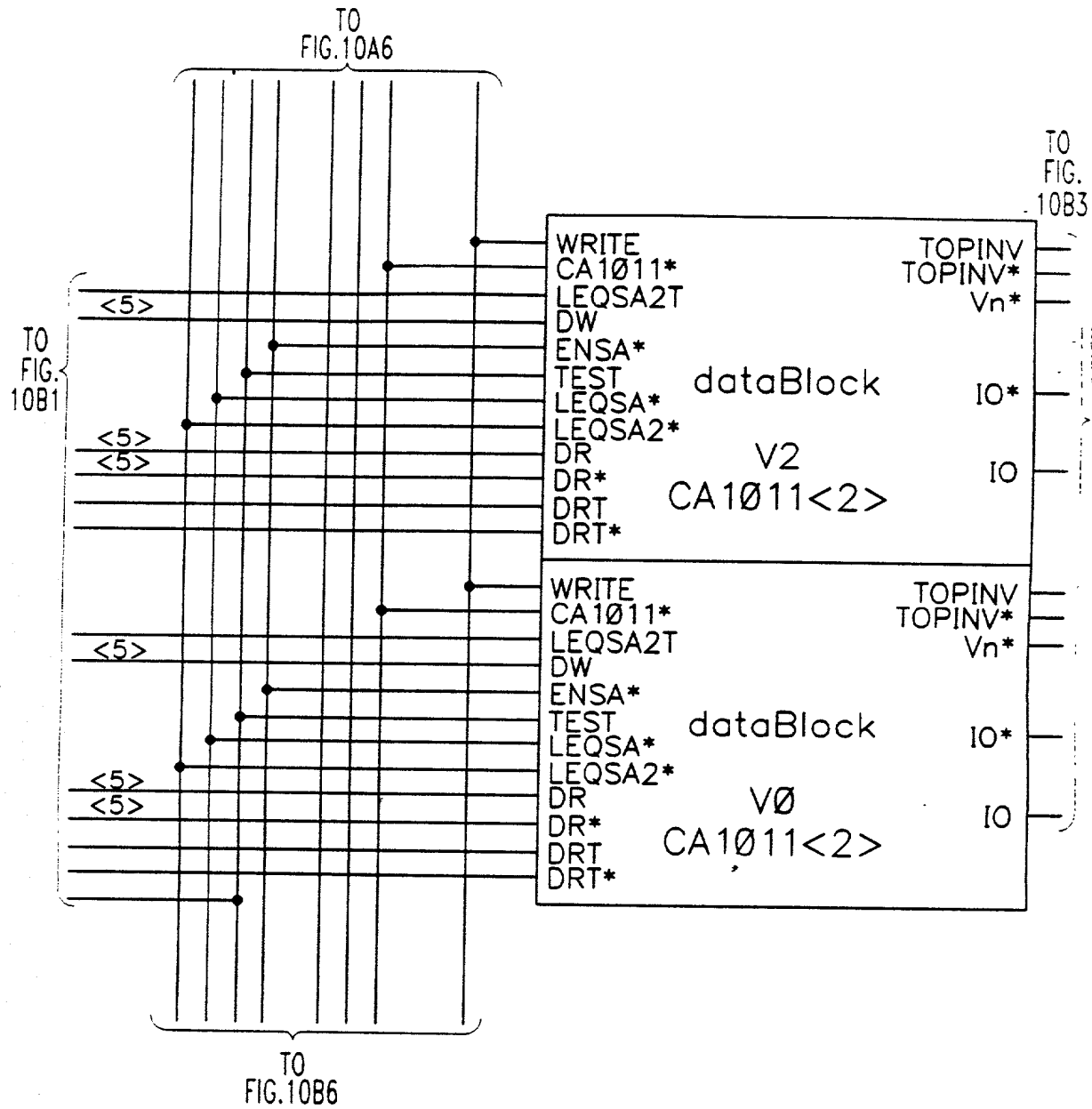


FIG. 10B2

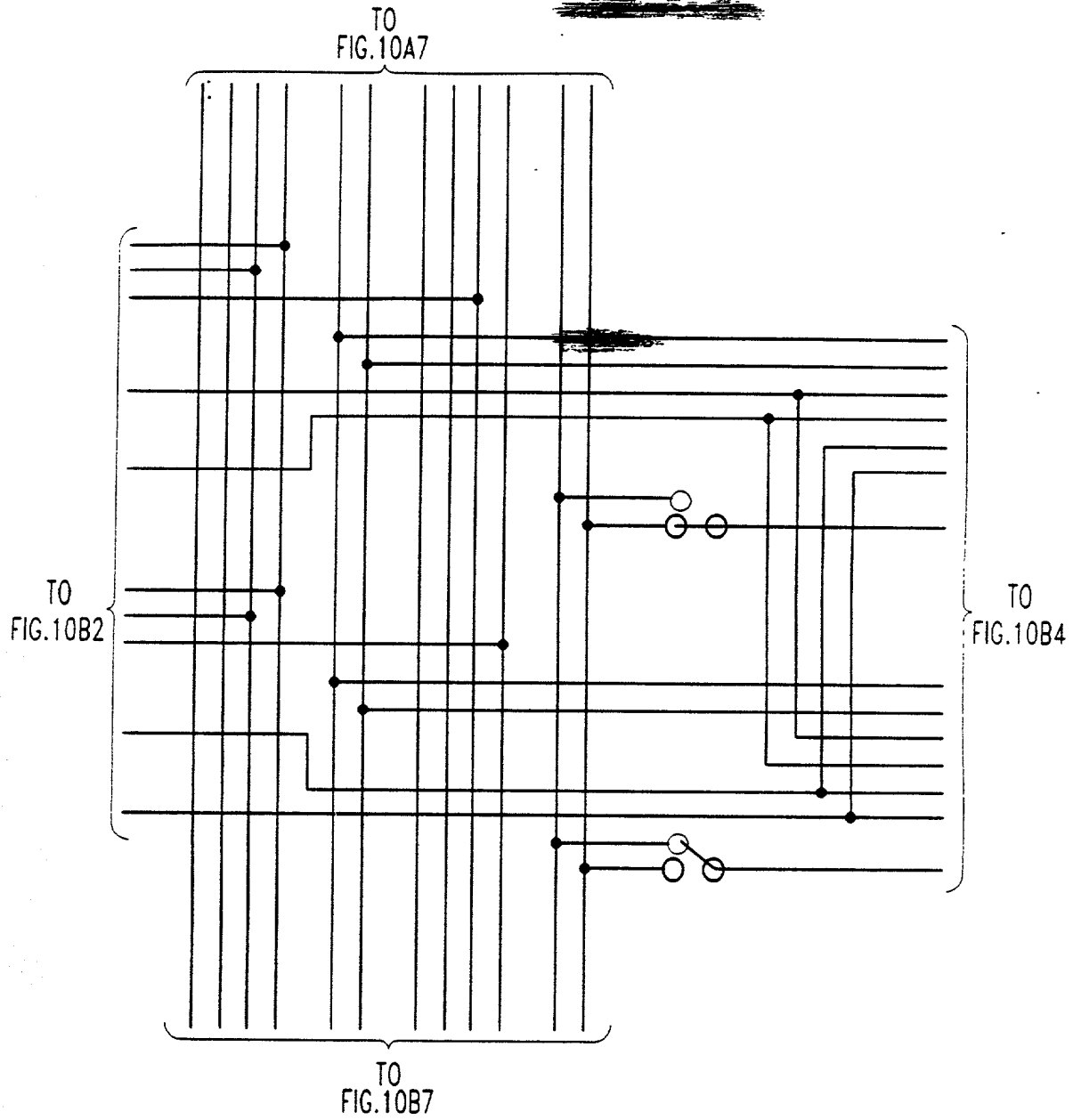


FIG. 10B3

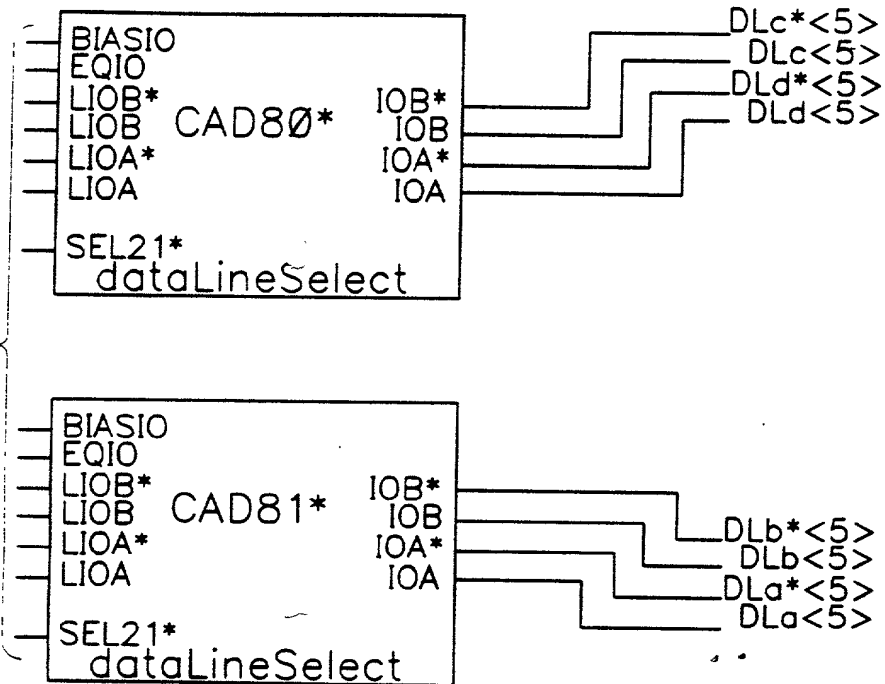
I/O<sub>b</sub>TO  
FIG. 10B3

FIG. 10B4

FIG. 10B5

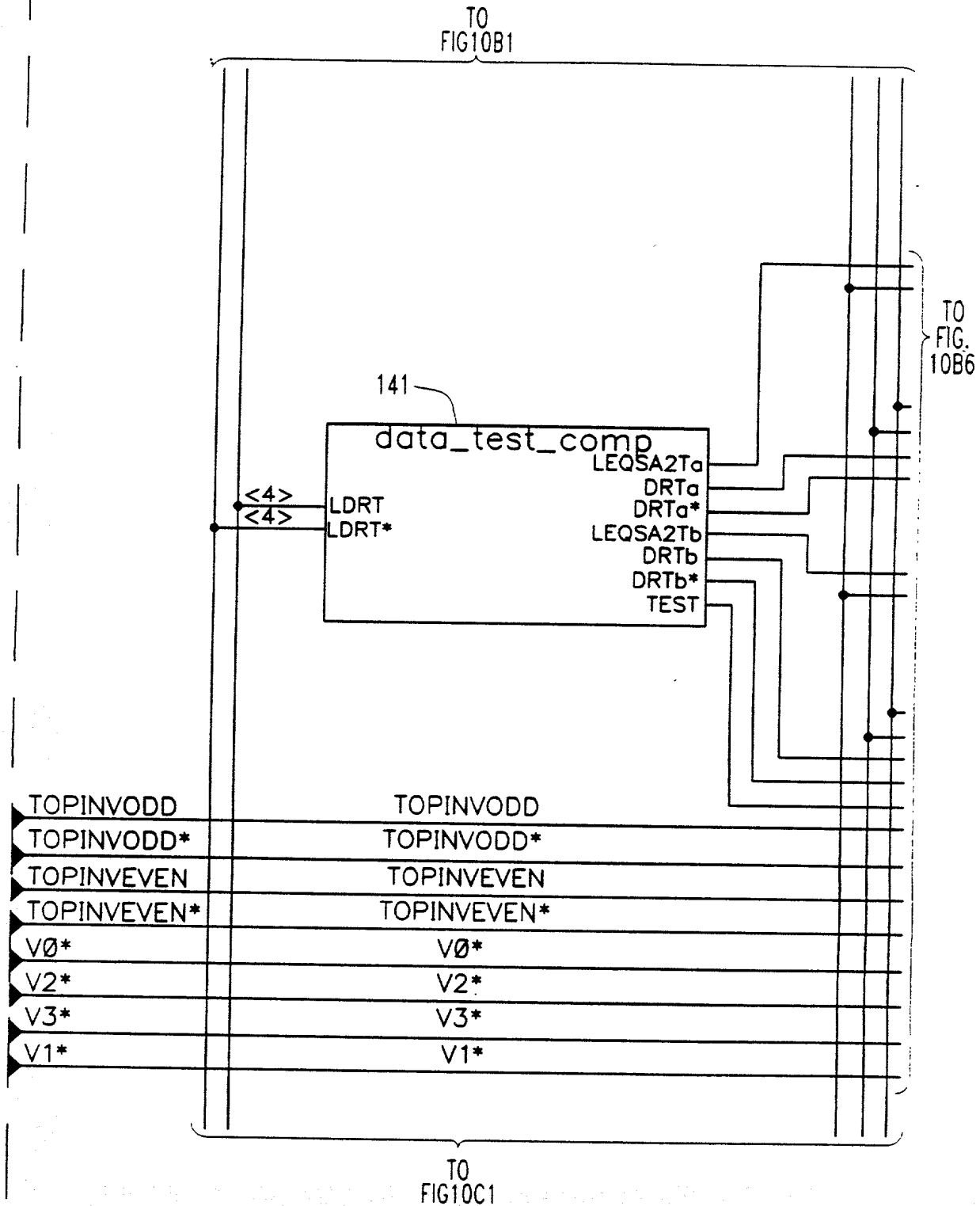


FIG. 10B6

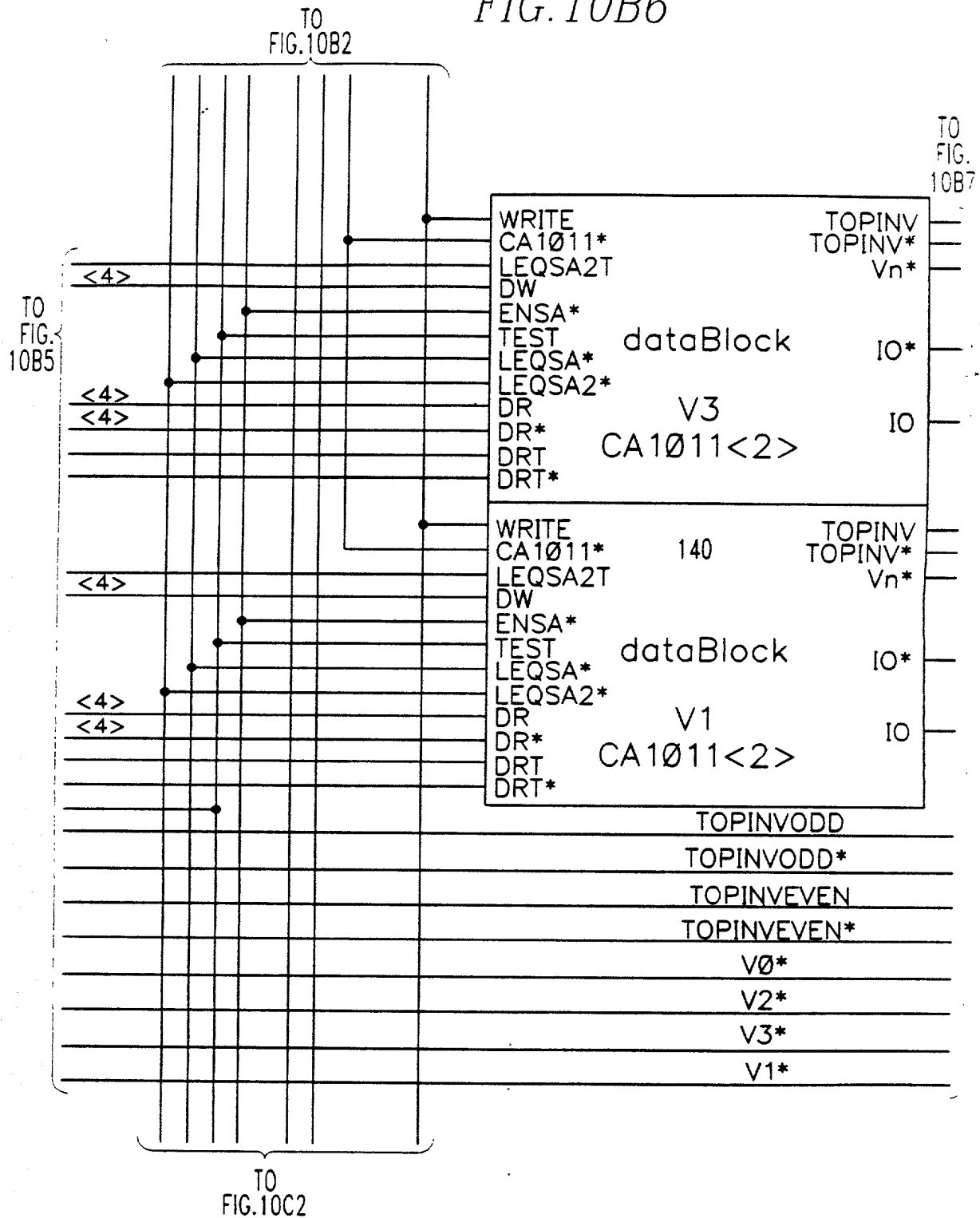


FIG. 10B7

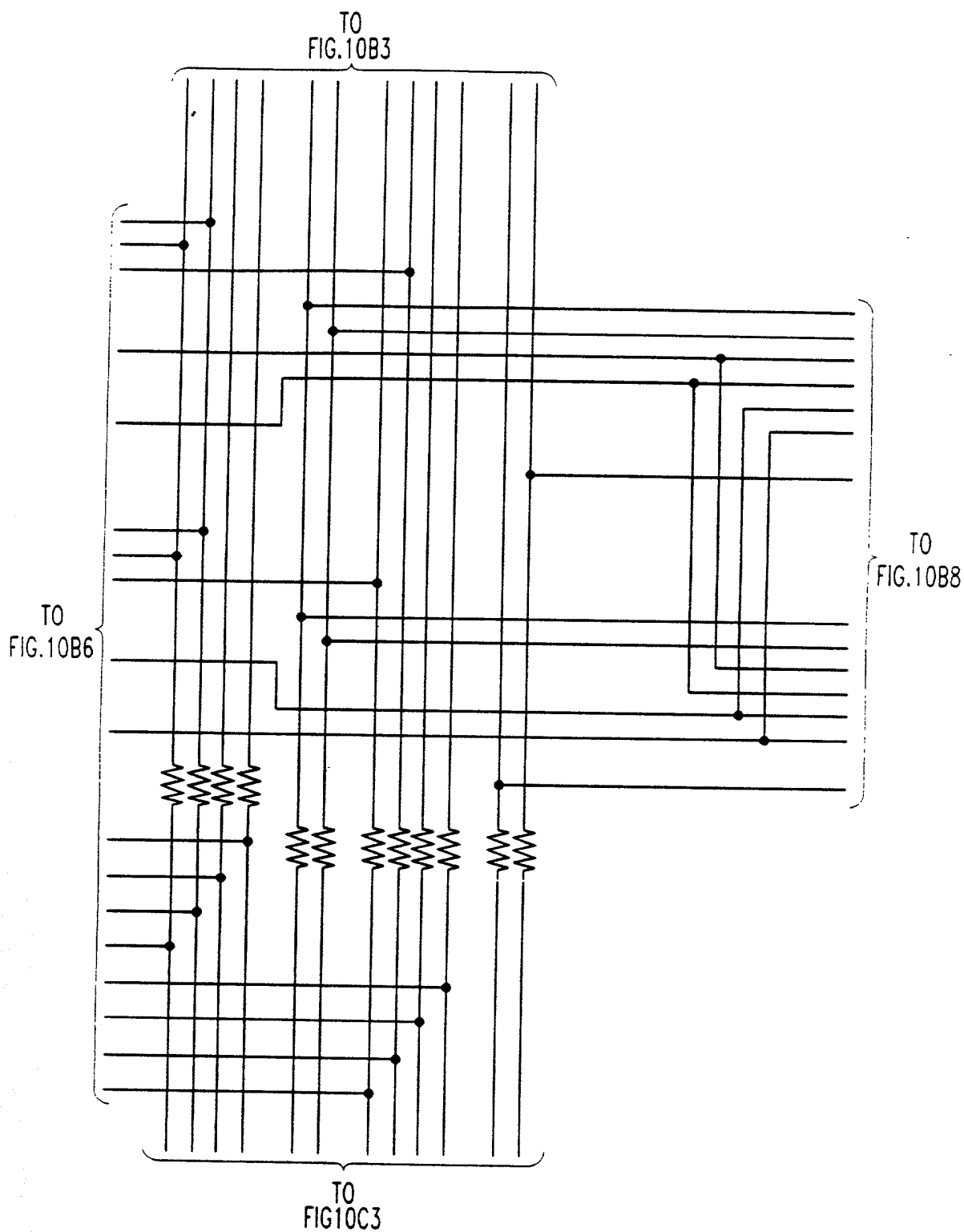
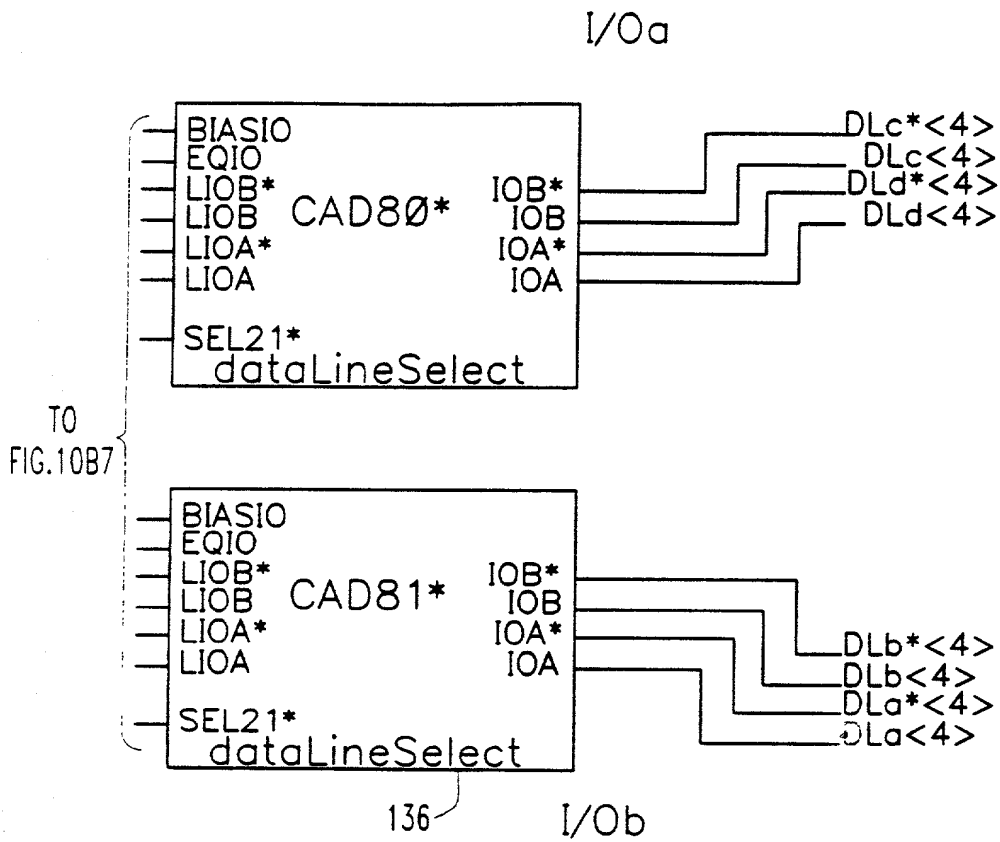


FIG. 10B8





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TO  
FIG.10B5

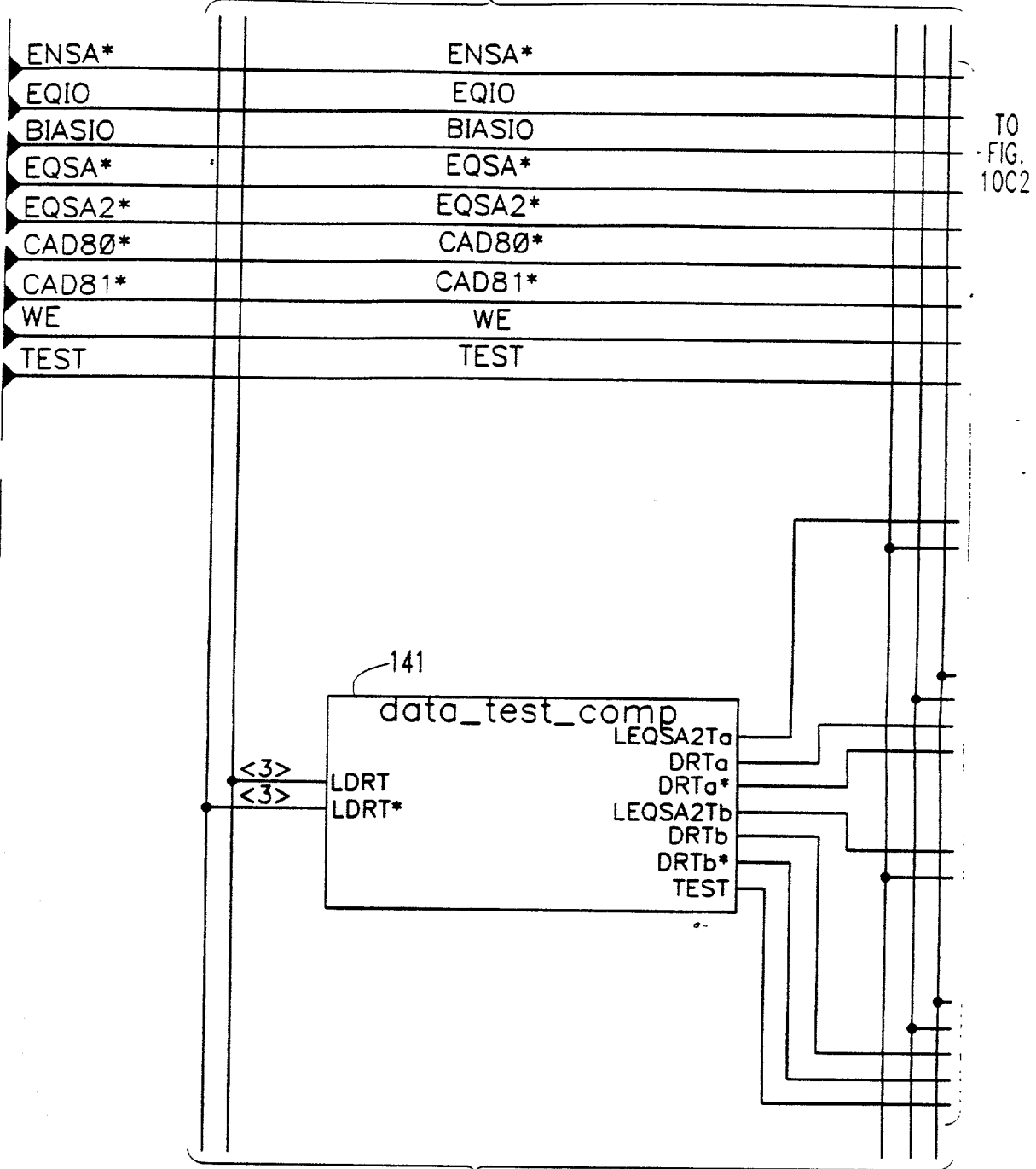


FIG. 10C1

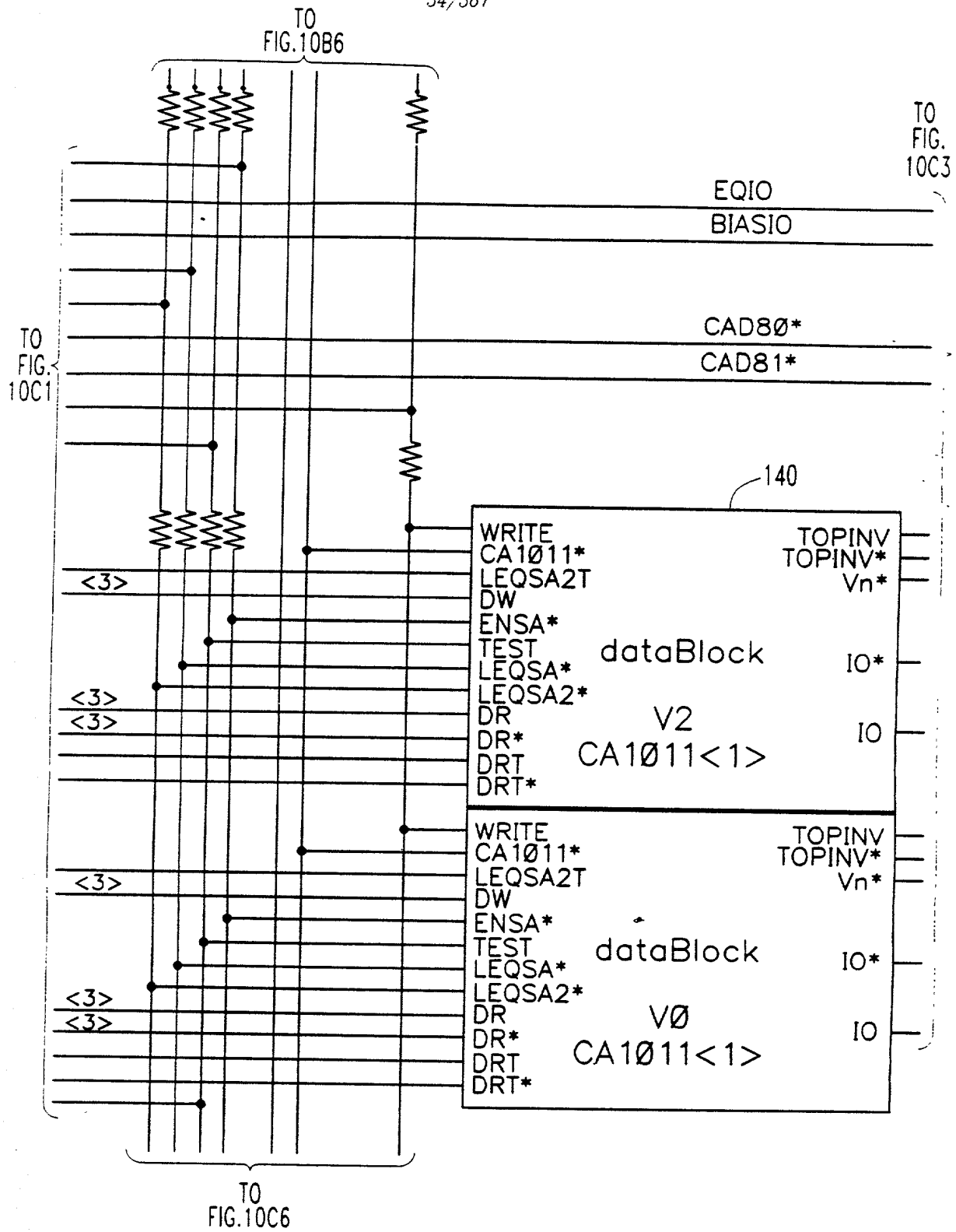


FIG. 10C2

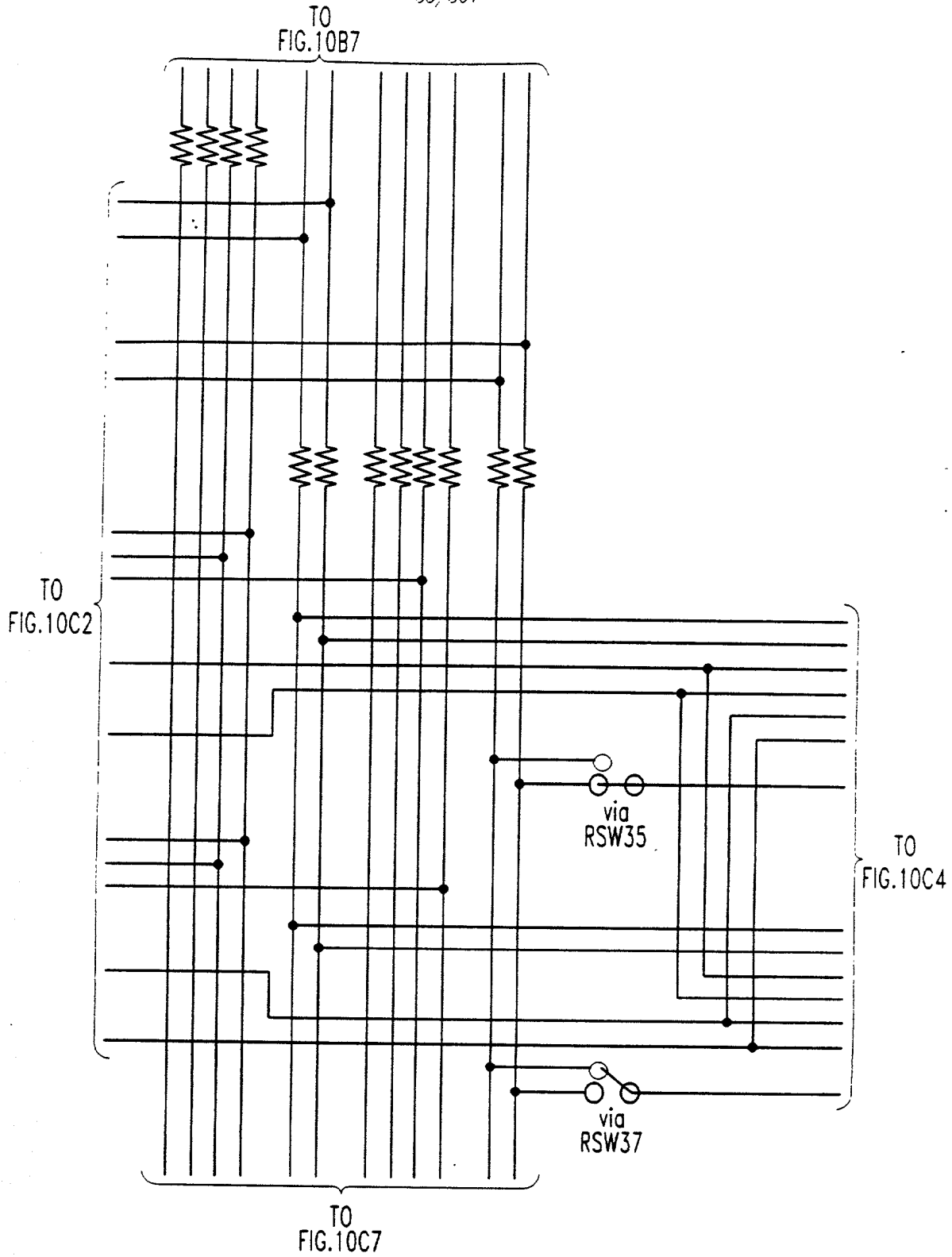
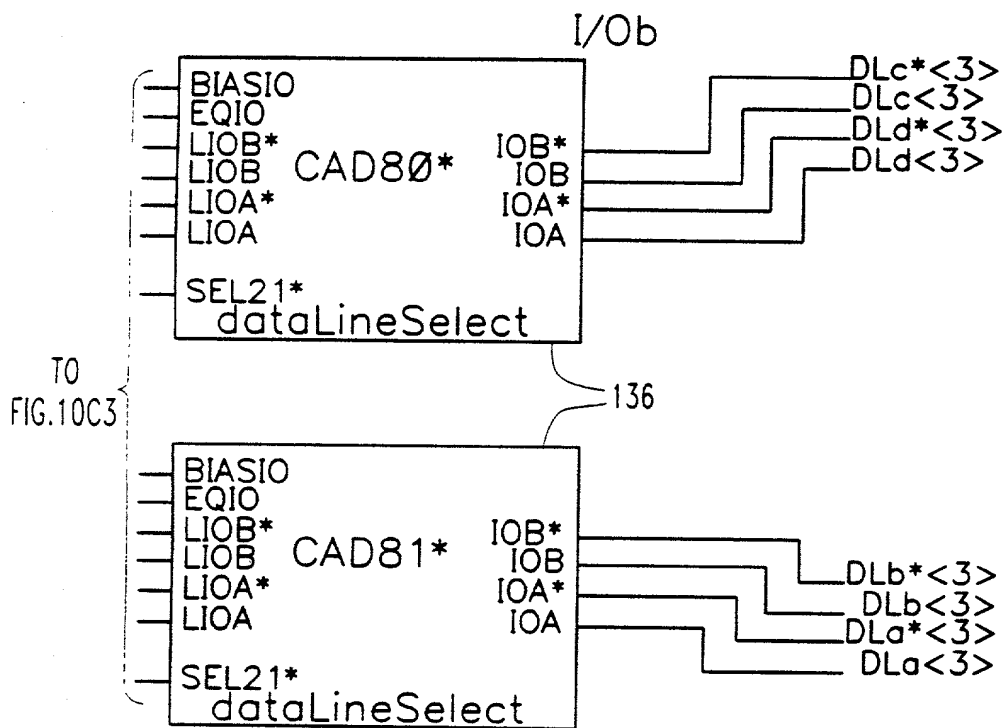


FIG. 10C3

FIG. 10C4



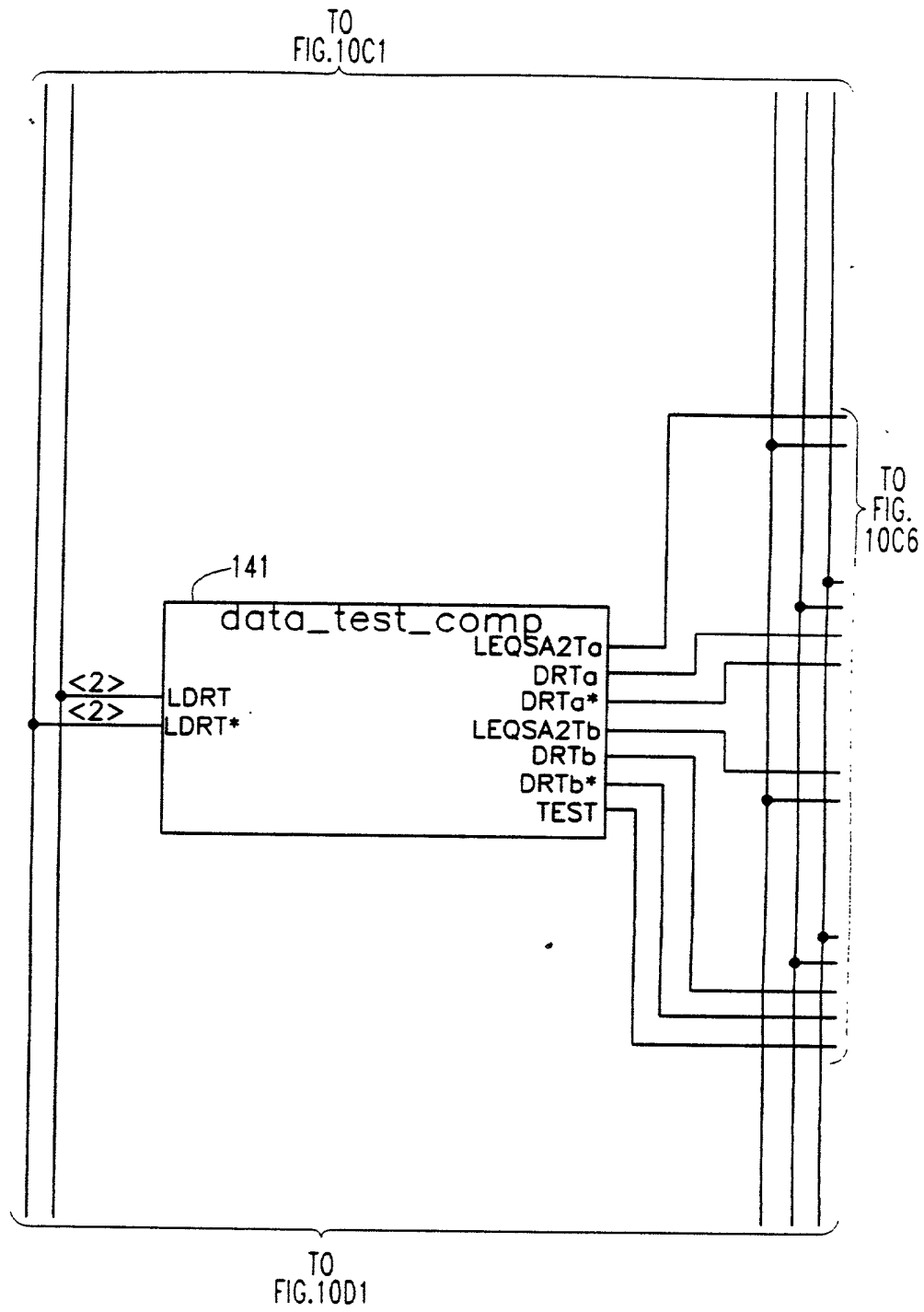


FIG.10C5

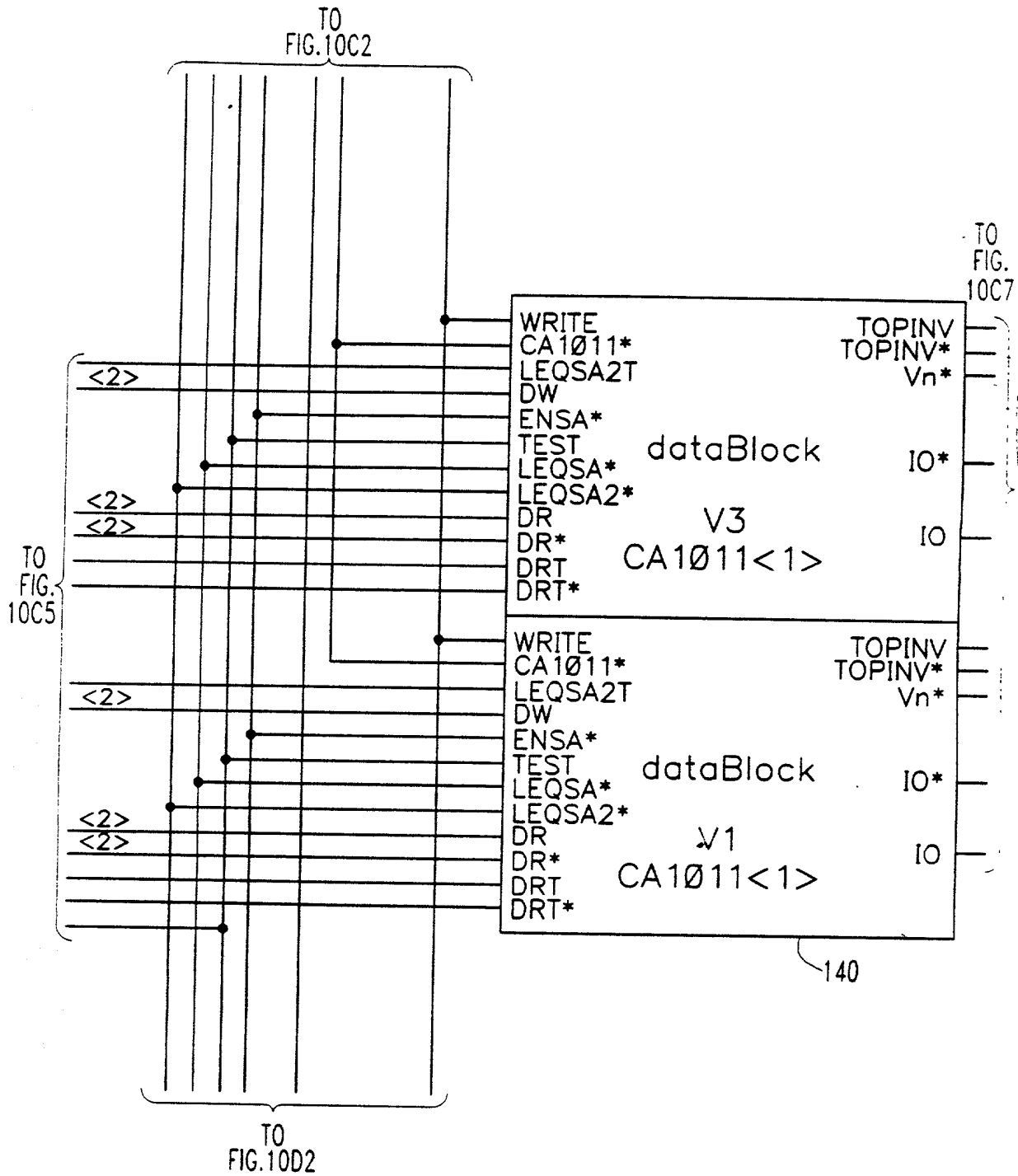


FIG. 10C6

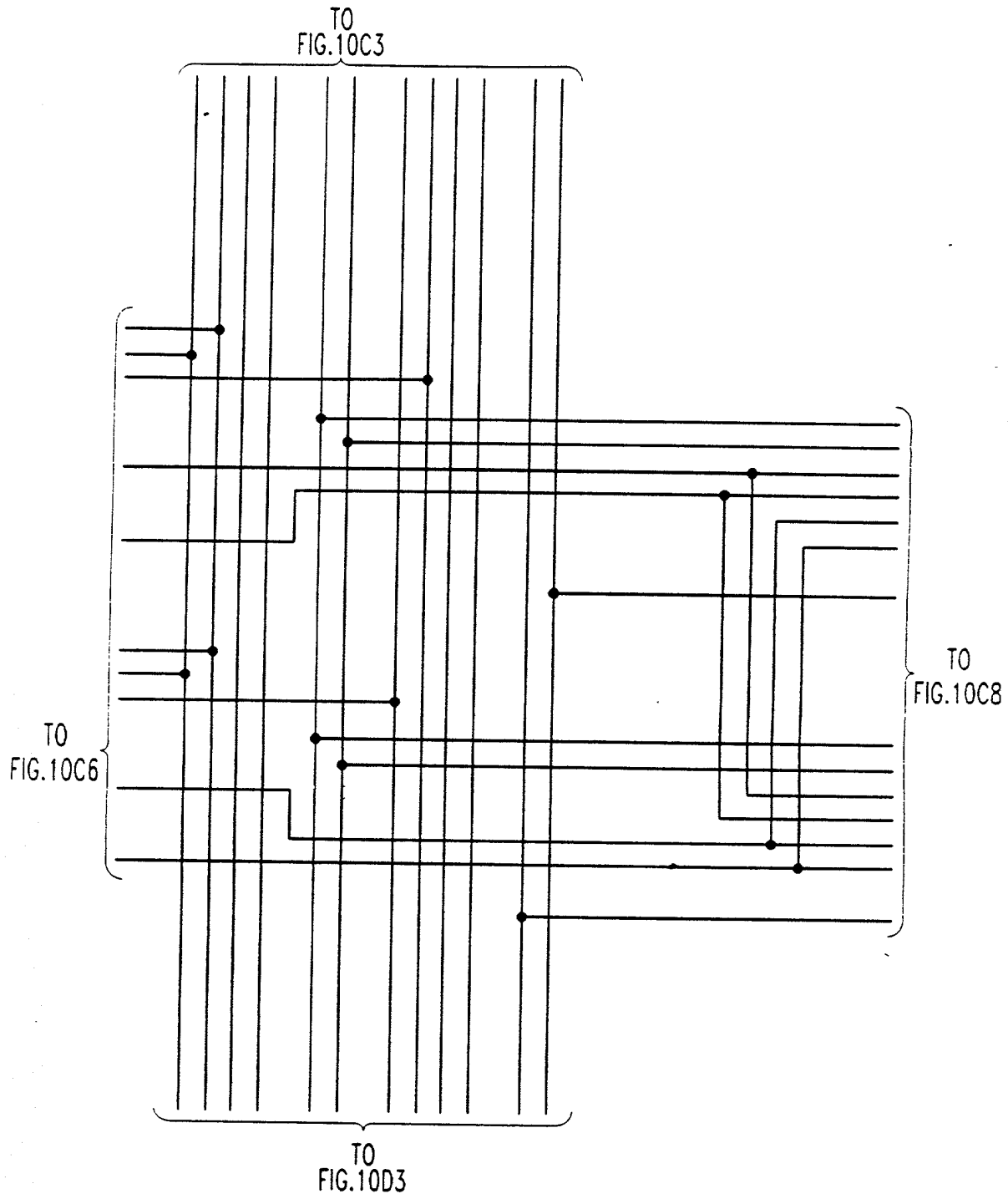


FIG. 10C7

I/Oa

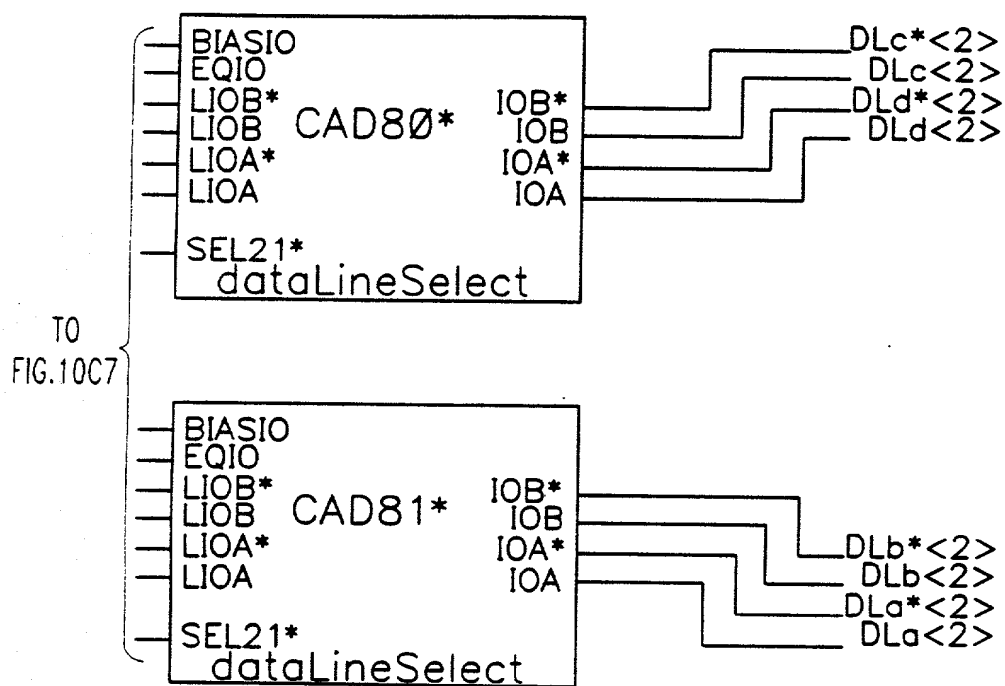


FIG.10C8



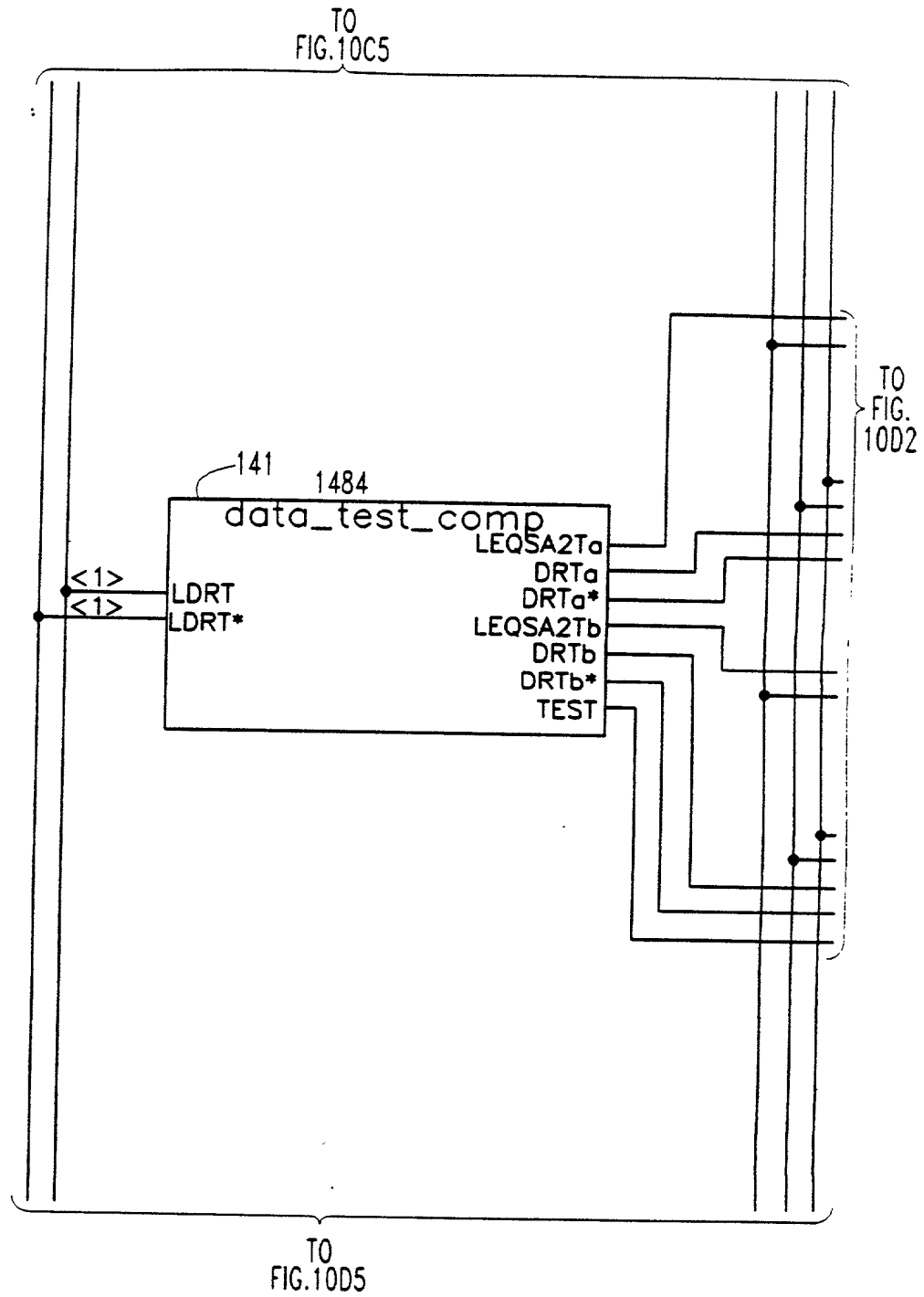


FIG.10D1

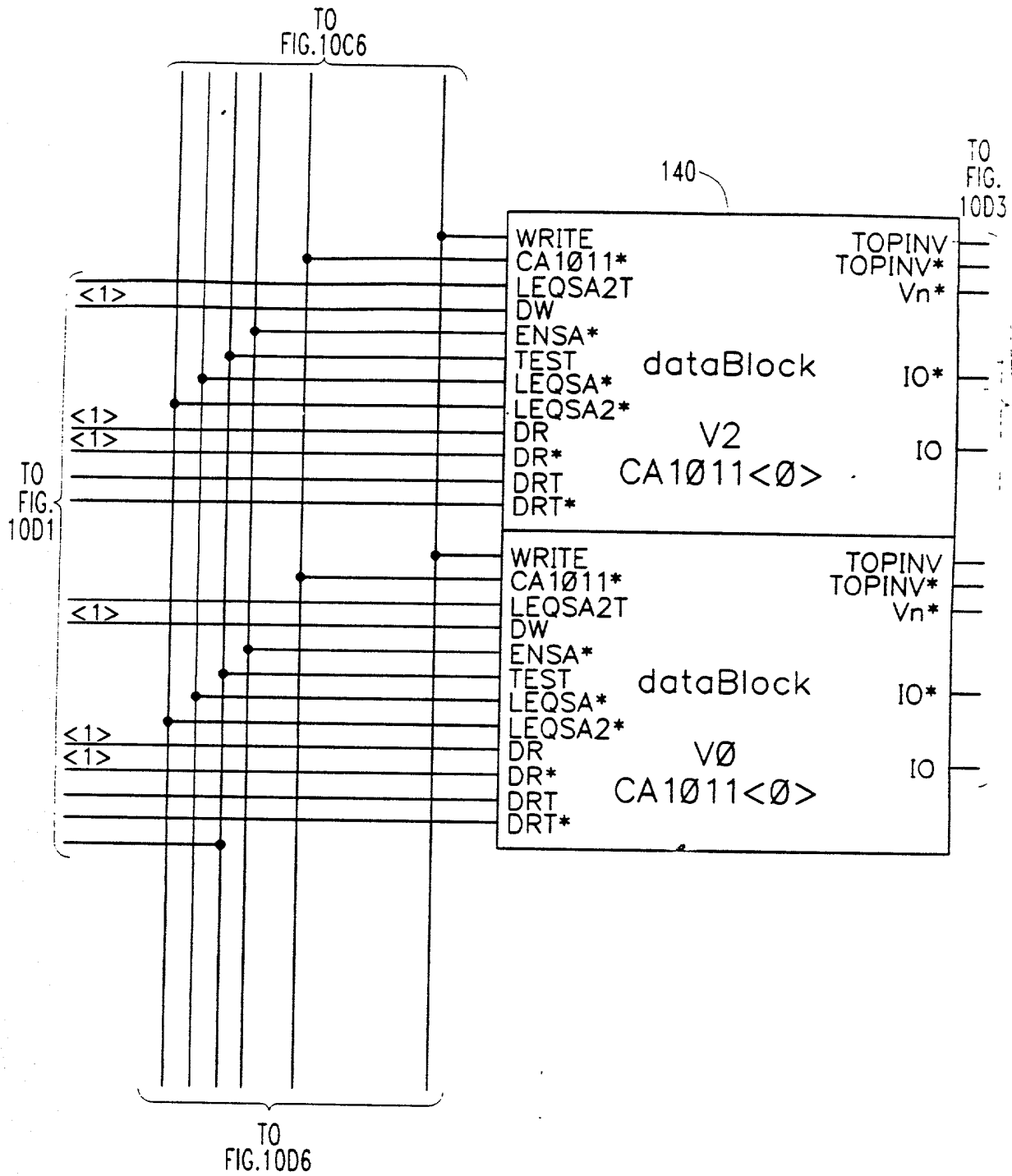


FIG. 10D2

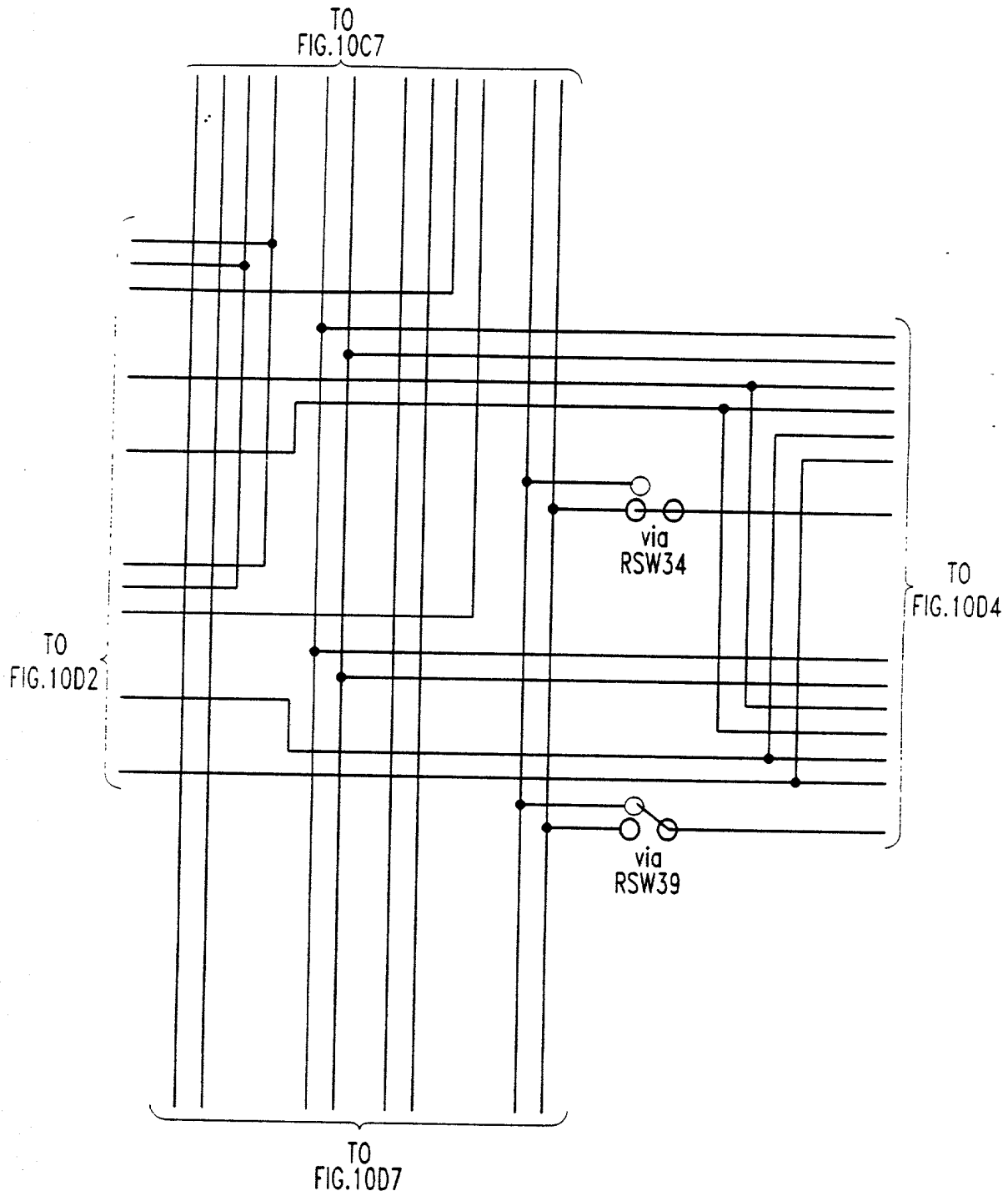


FIG. 10D3

I/Ob

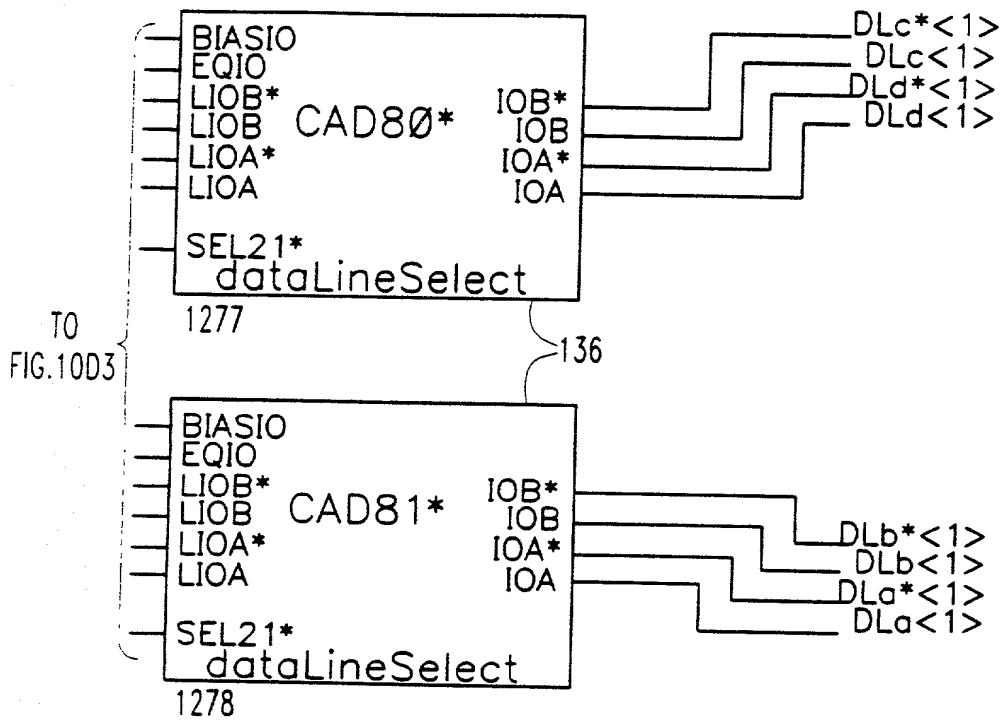


FIG. 10D4

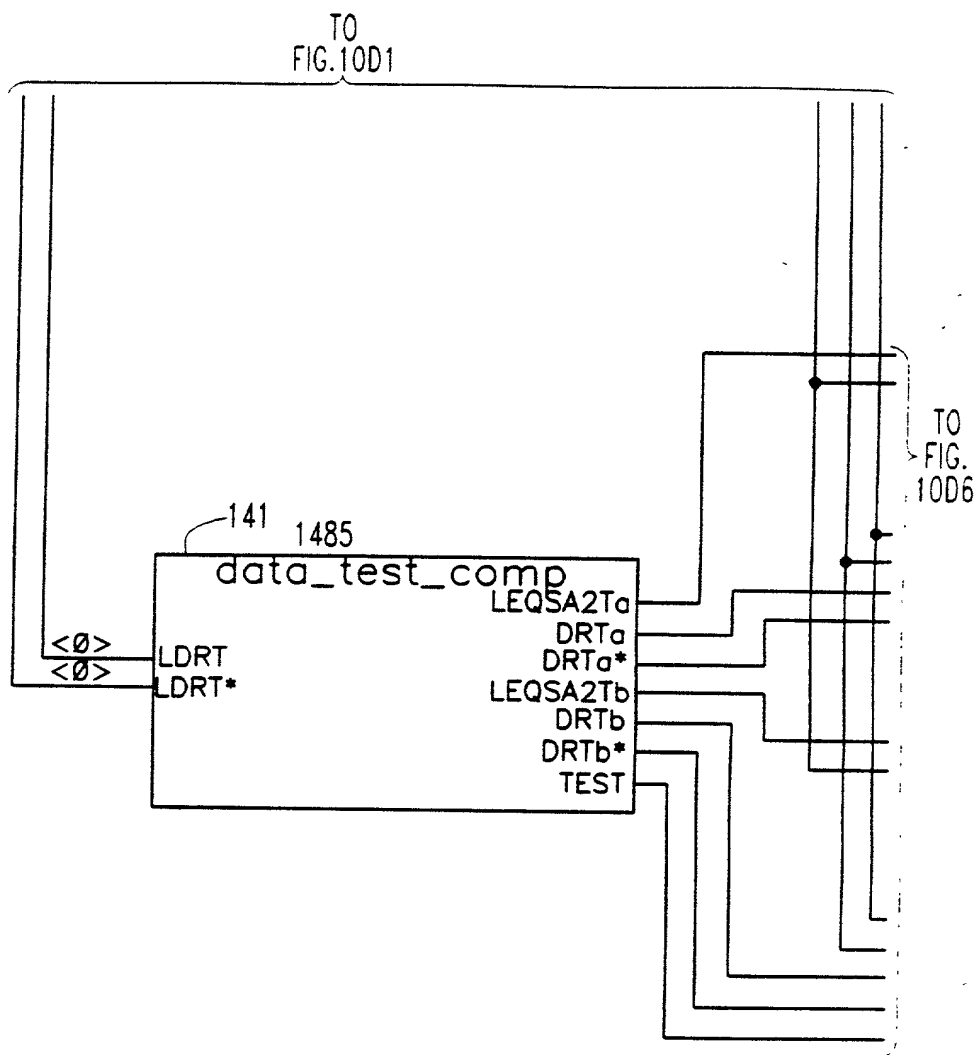


FIG. 10D5

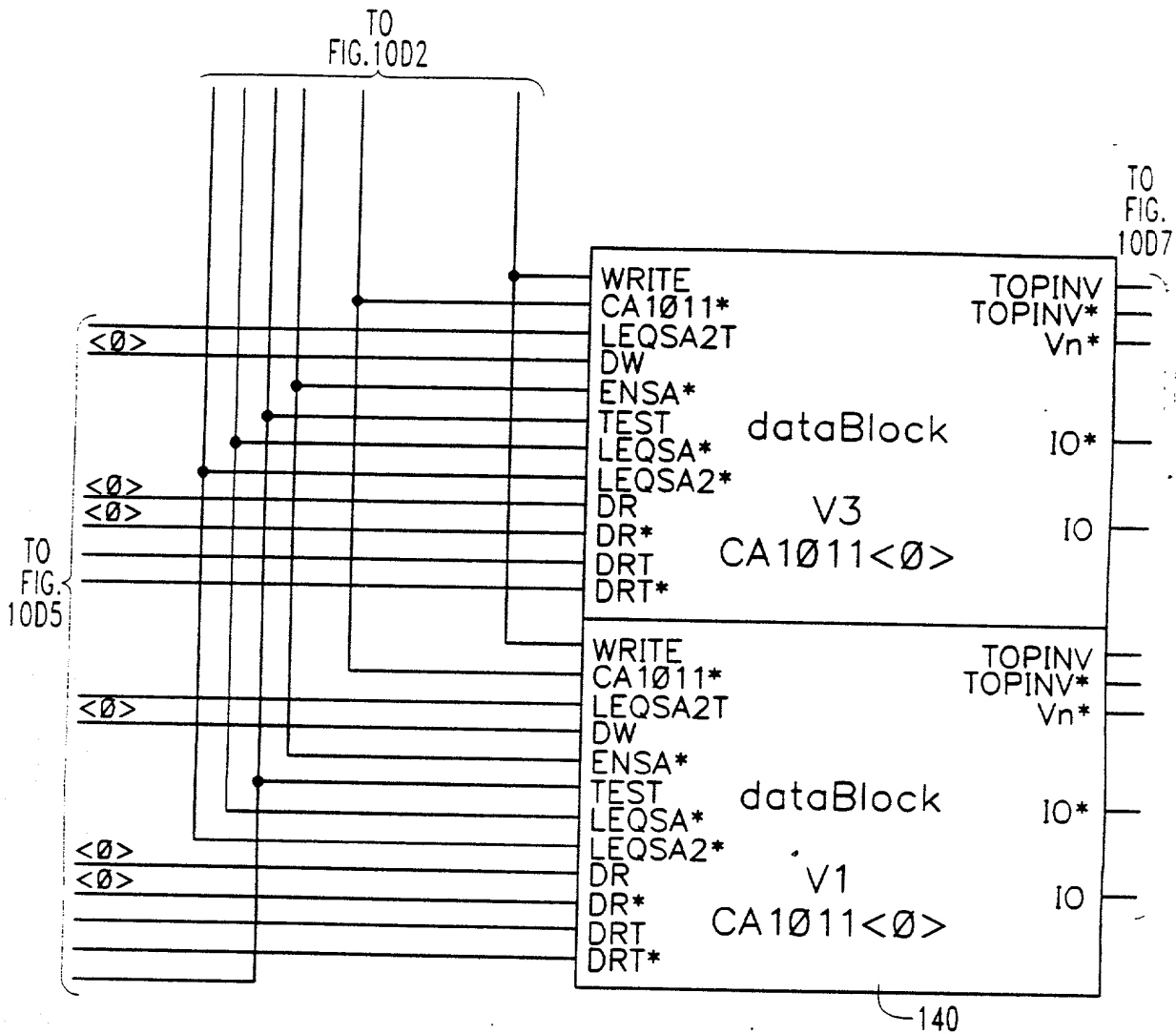


FIG. 10D6

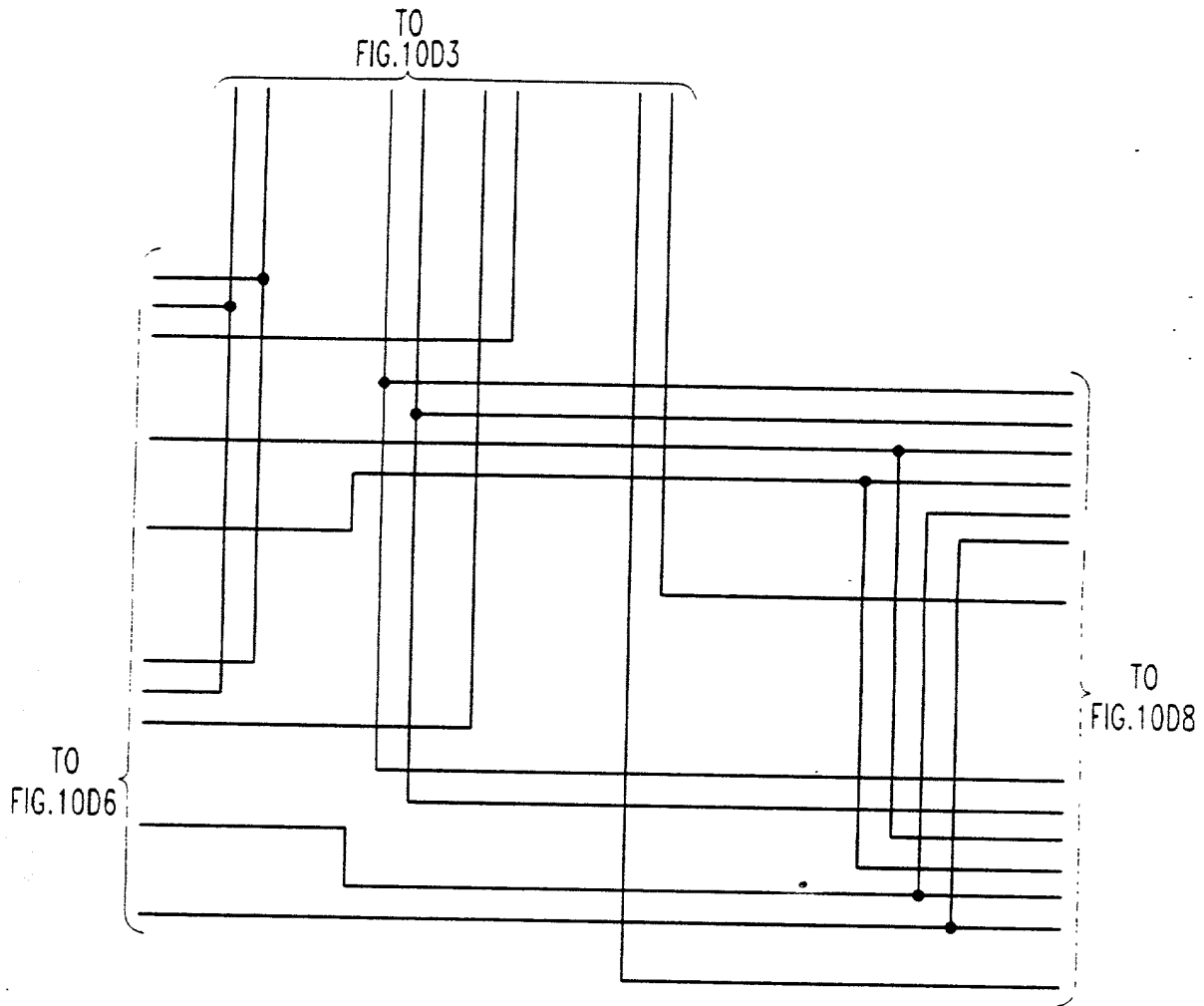
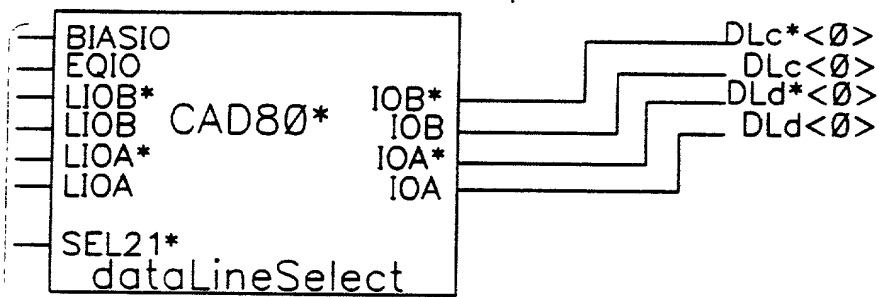
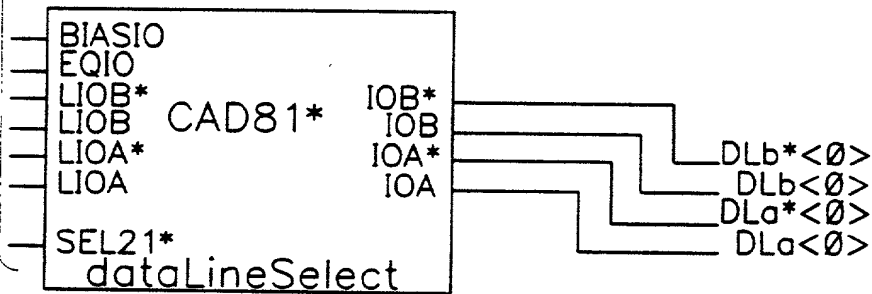


FIG. 10D7

I/Oa

TO  
FIG.10D7

I/Ob

FIG.10D8



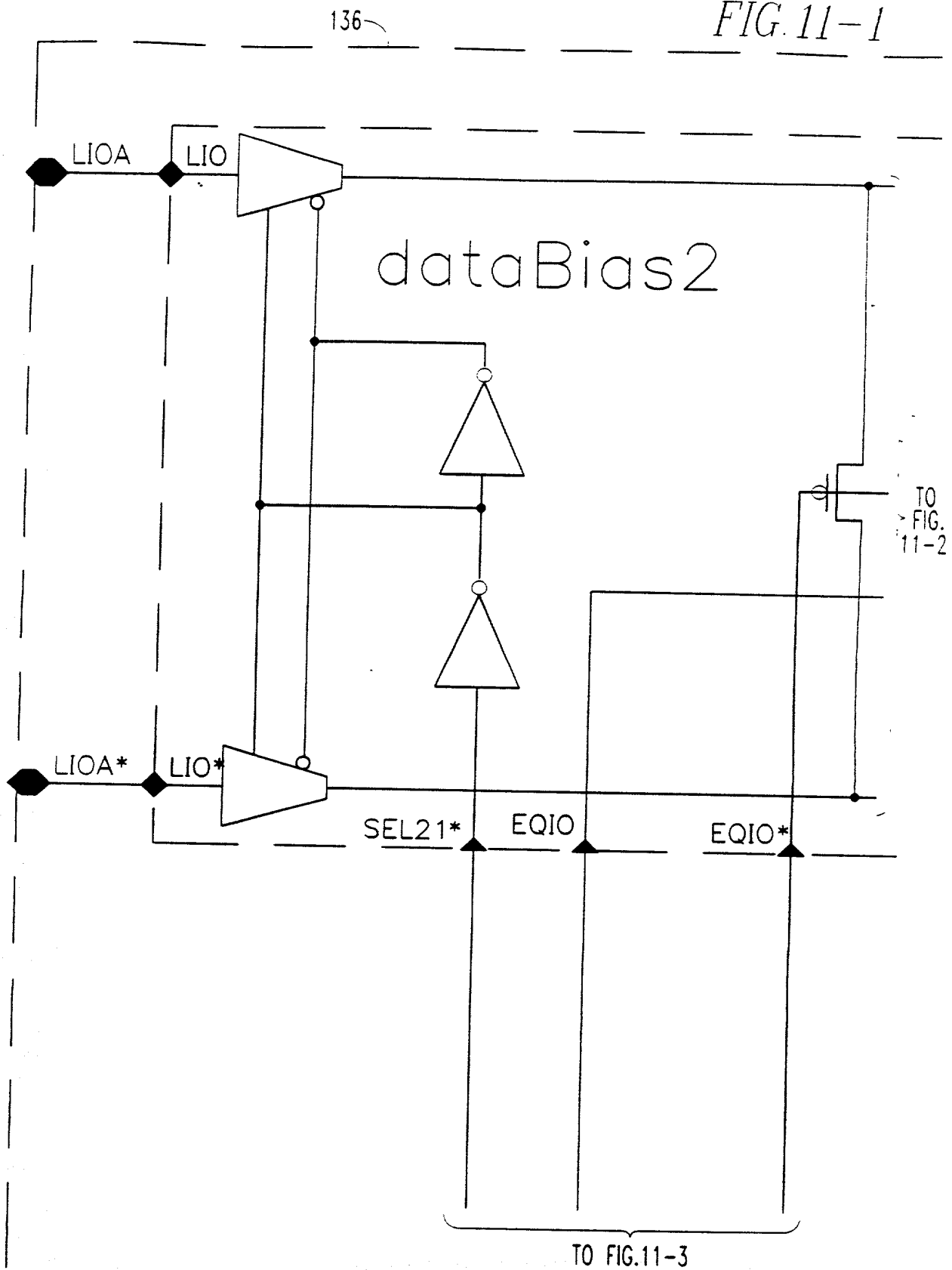
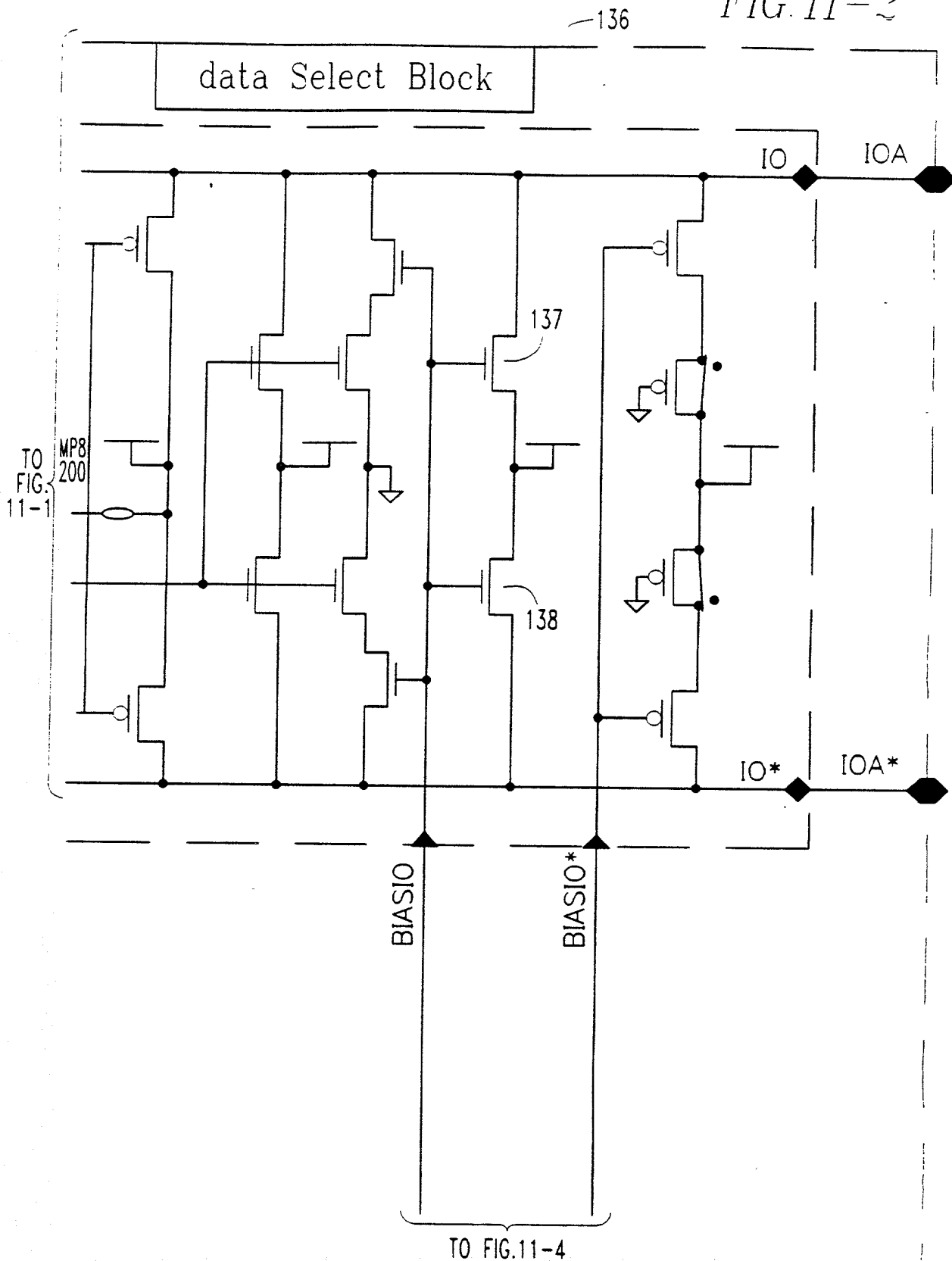


FIG. 11-2



51.367

TO FIG.11-1

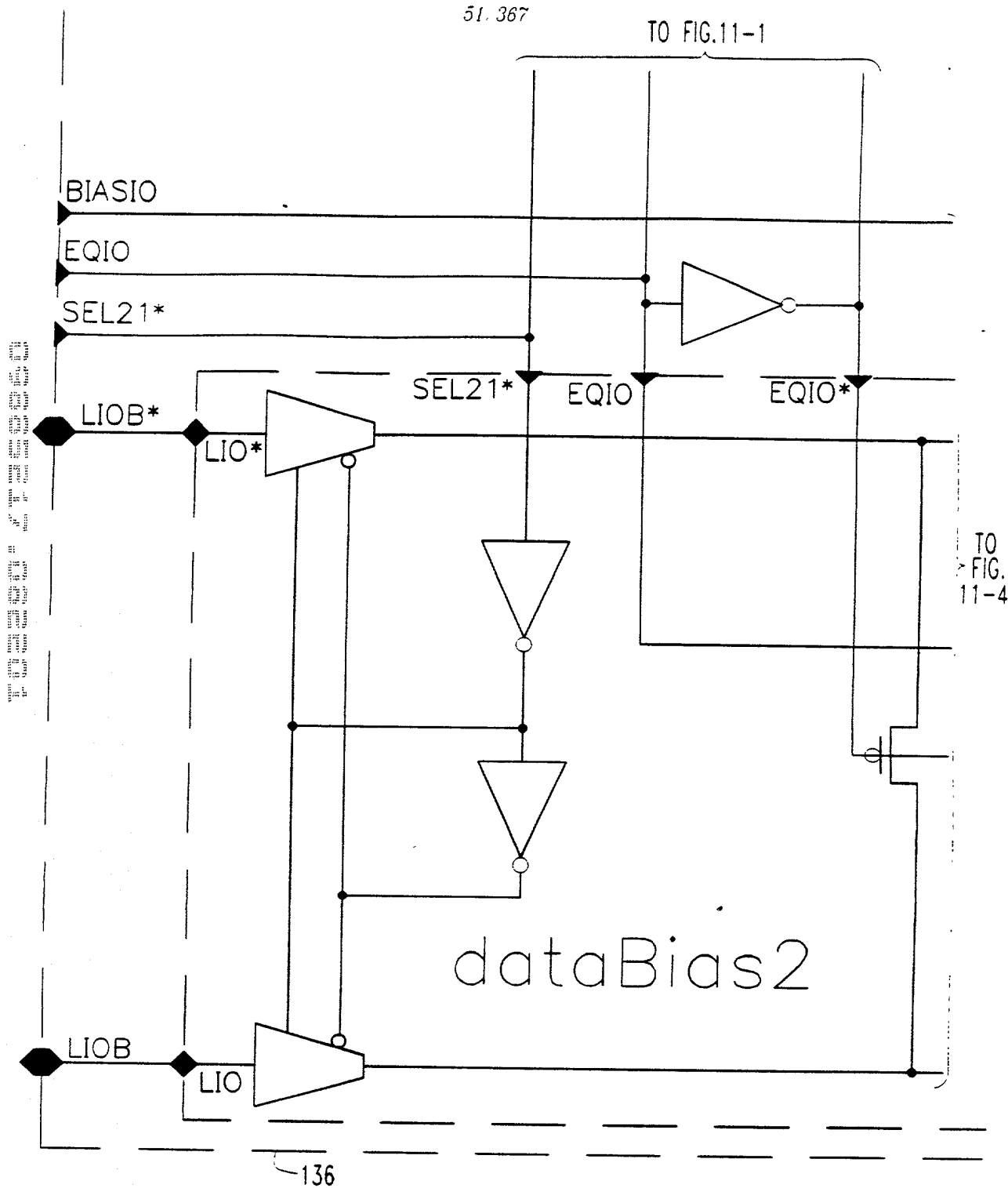
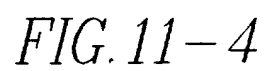


FIG.11-3



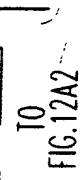
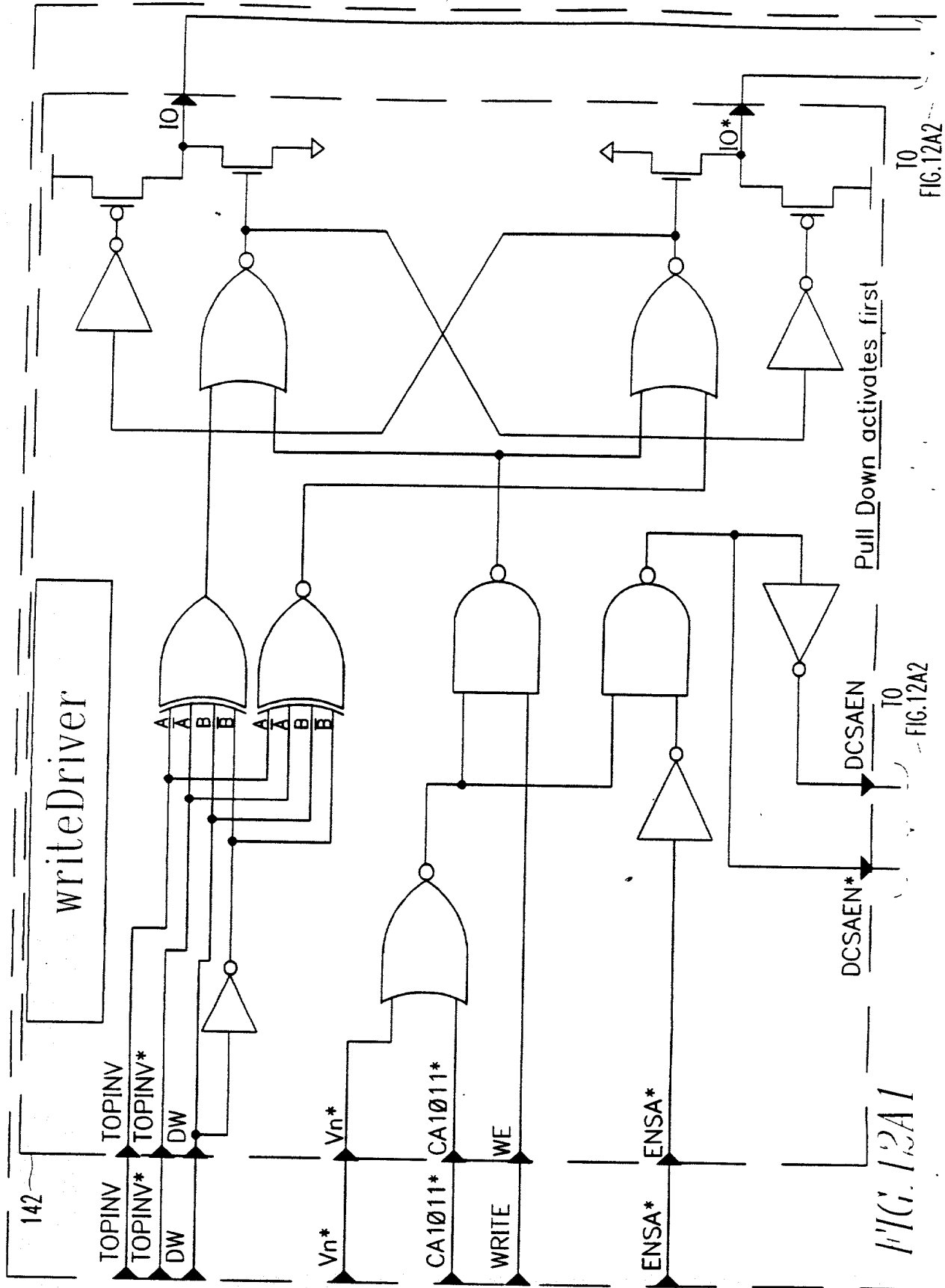


FIG. 12A1

FIG. 12A1

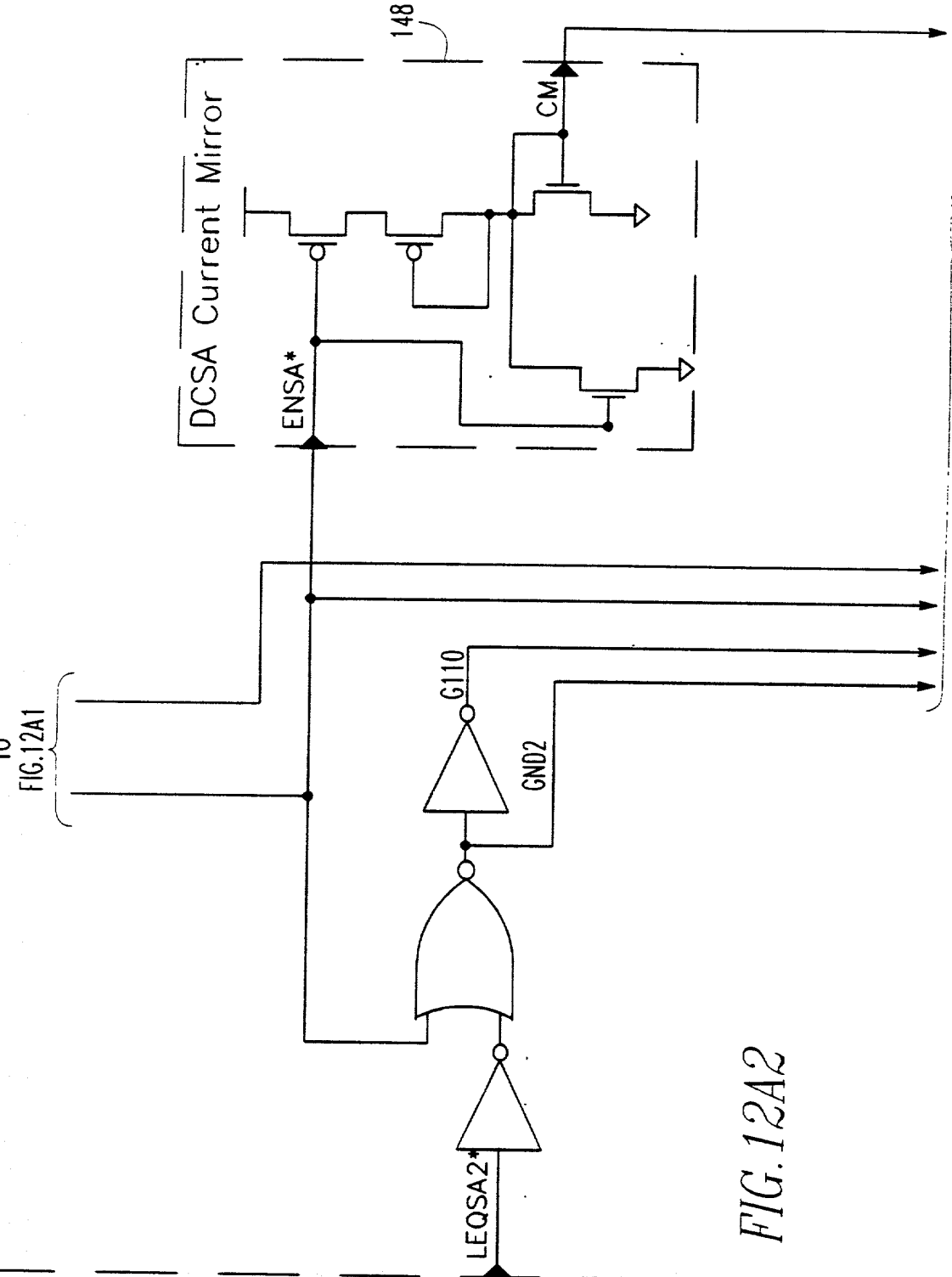
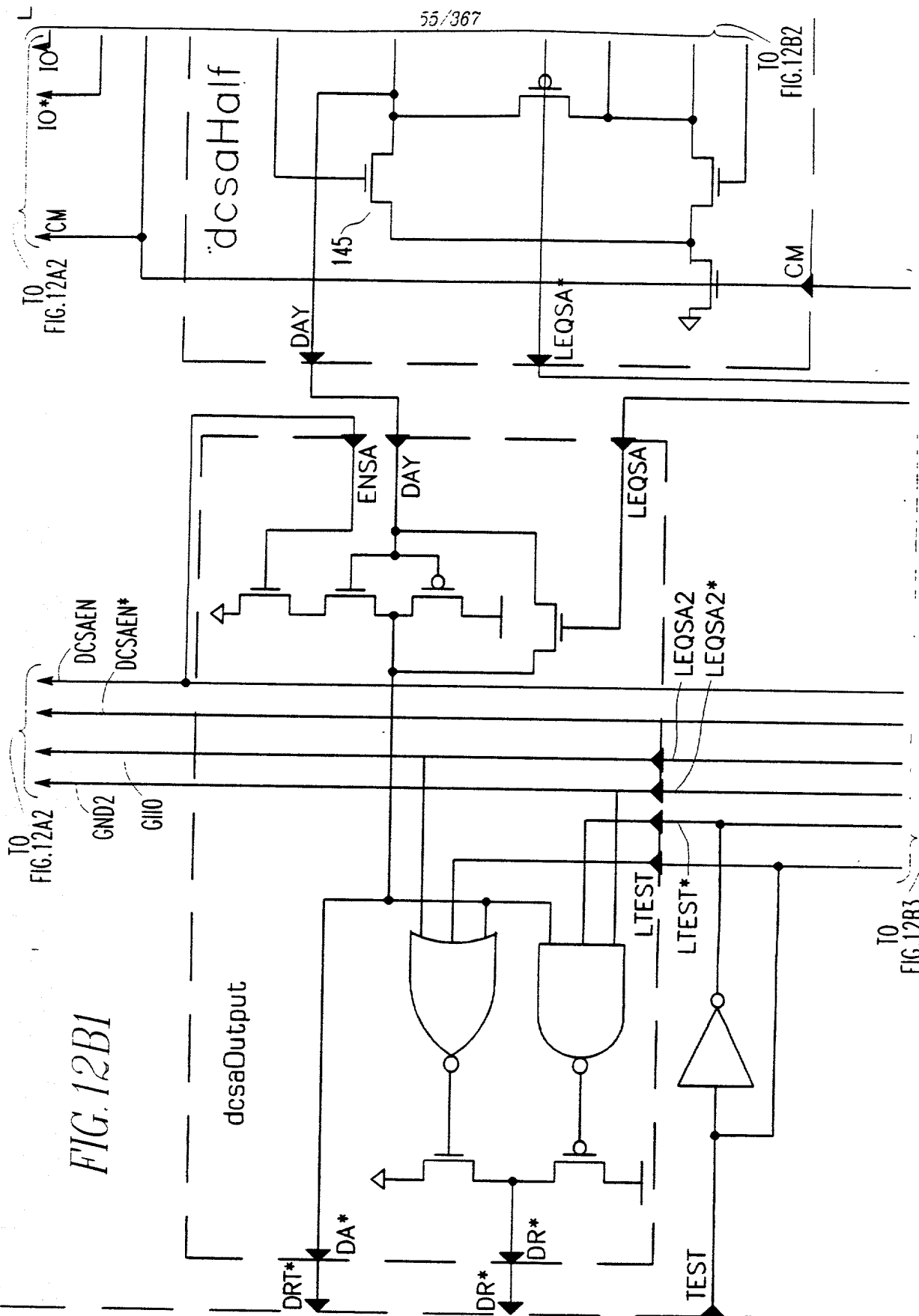


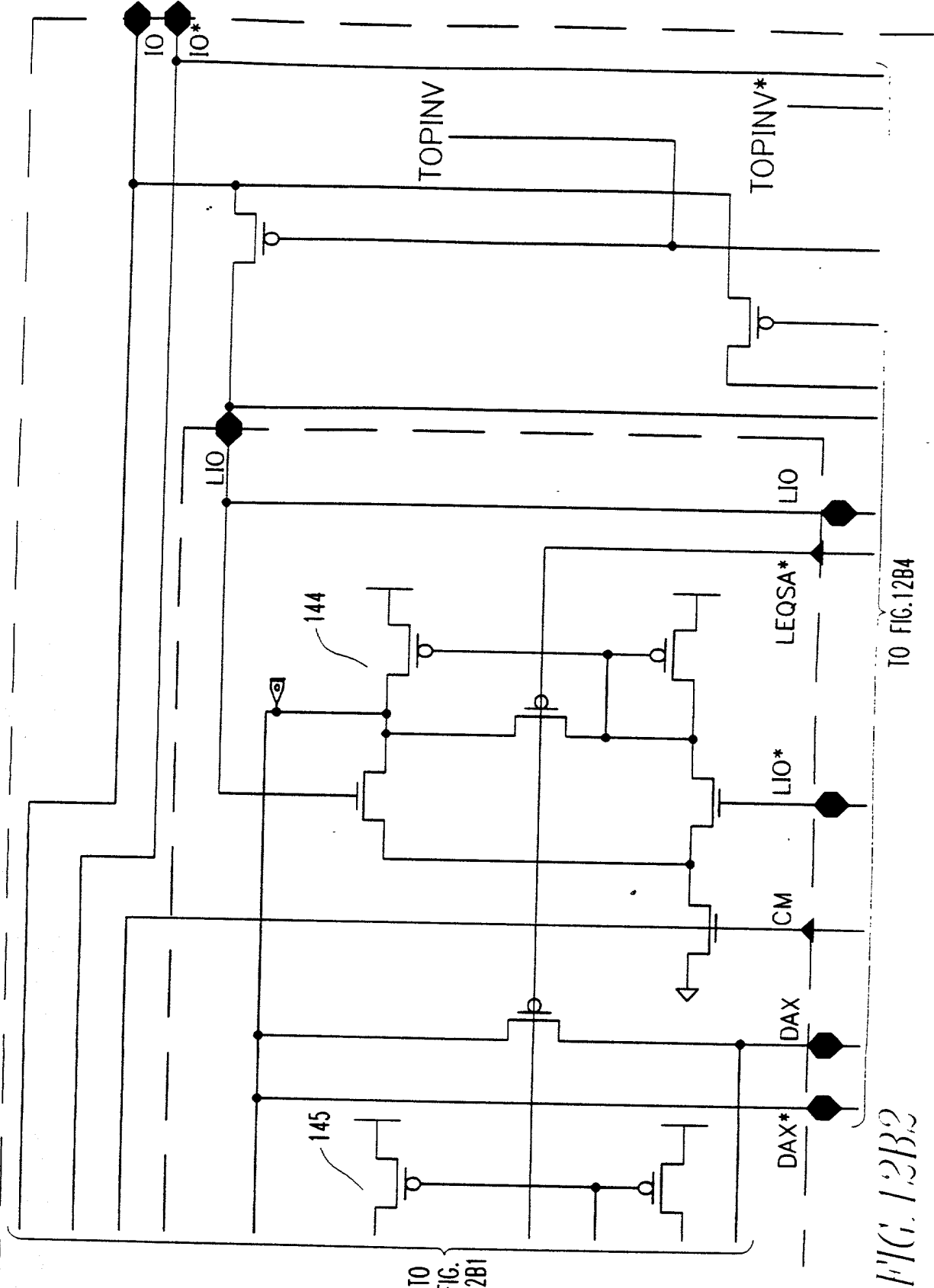
FIG. 12A2

FIG. 12B1

FIG. 12B1

FIG. 12B1





TO FIG. 12B4

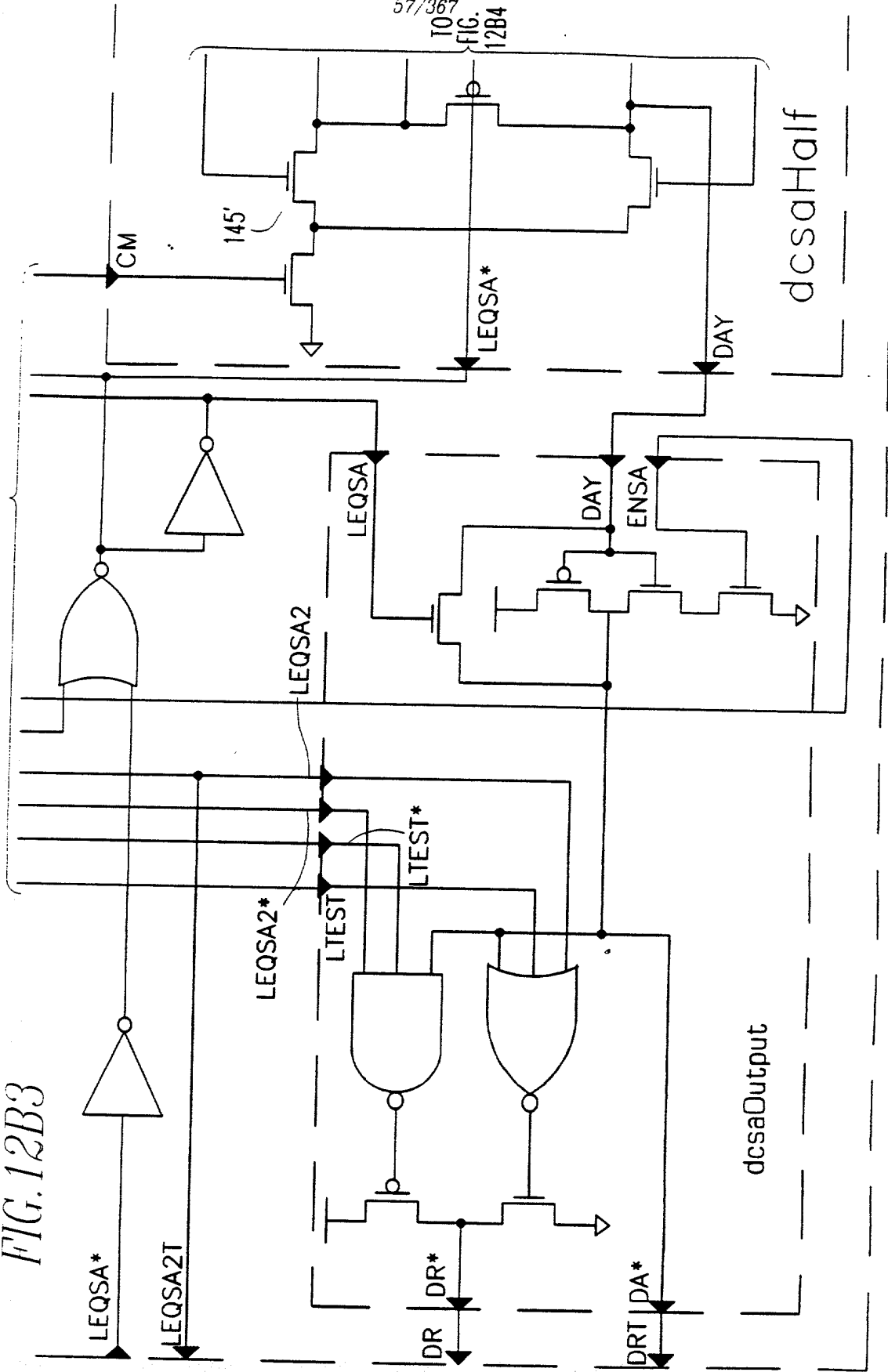
FIG. 12B2

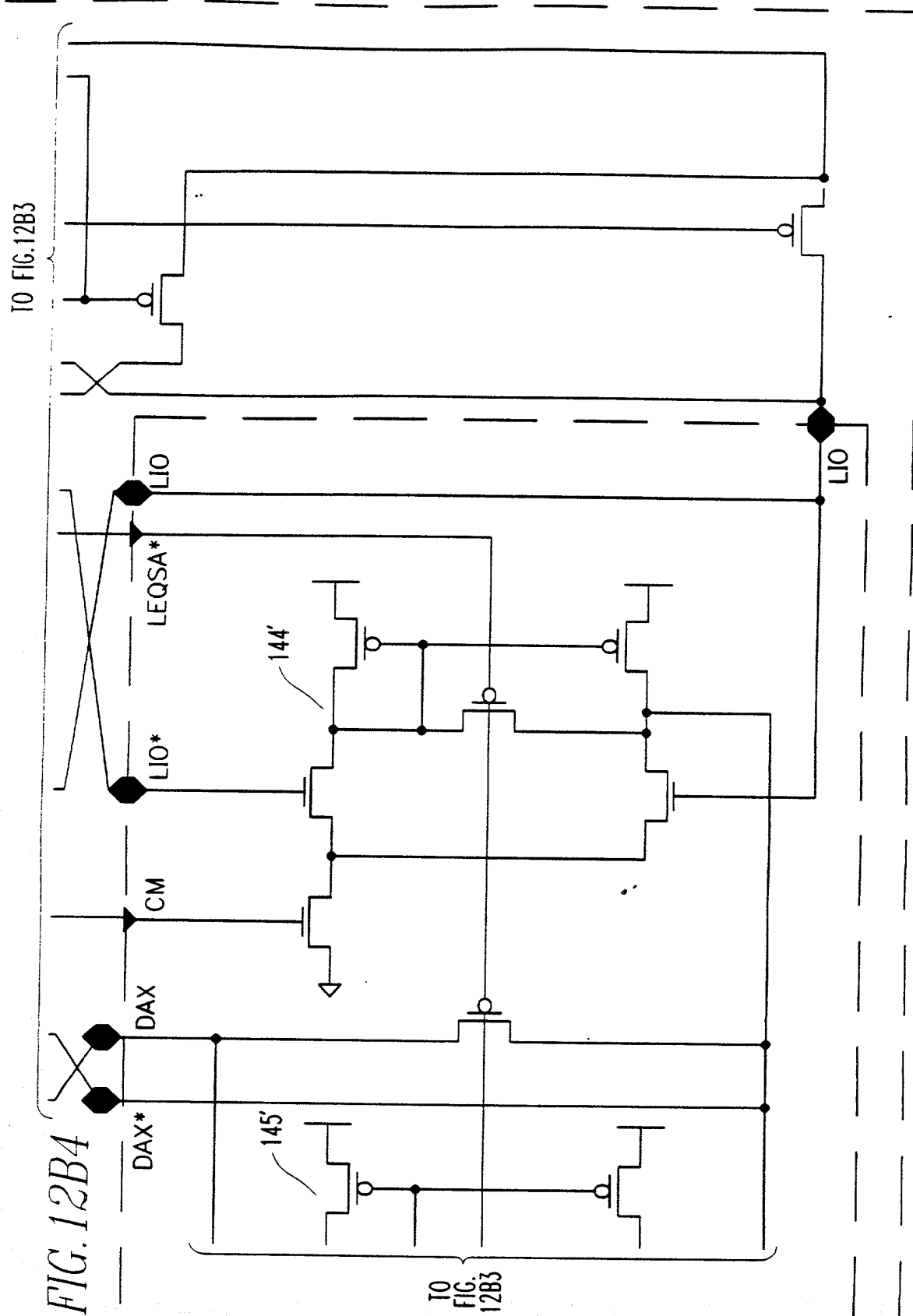
FIG. 12B1

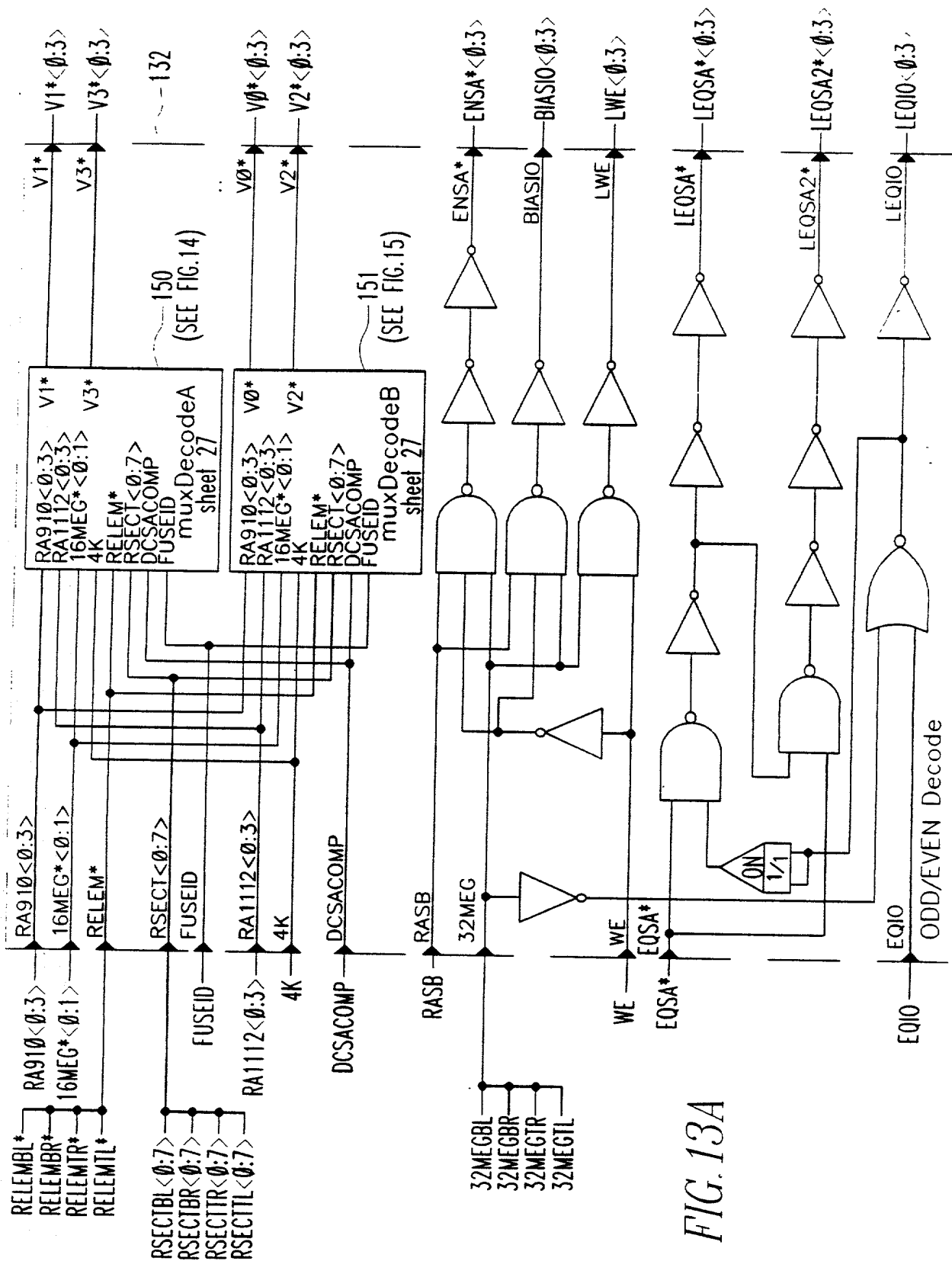


FIG. 12B3

TO FIG. 12B1







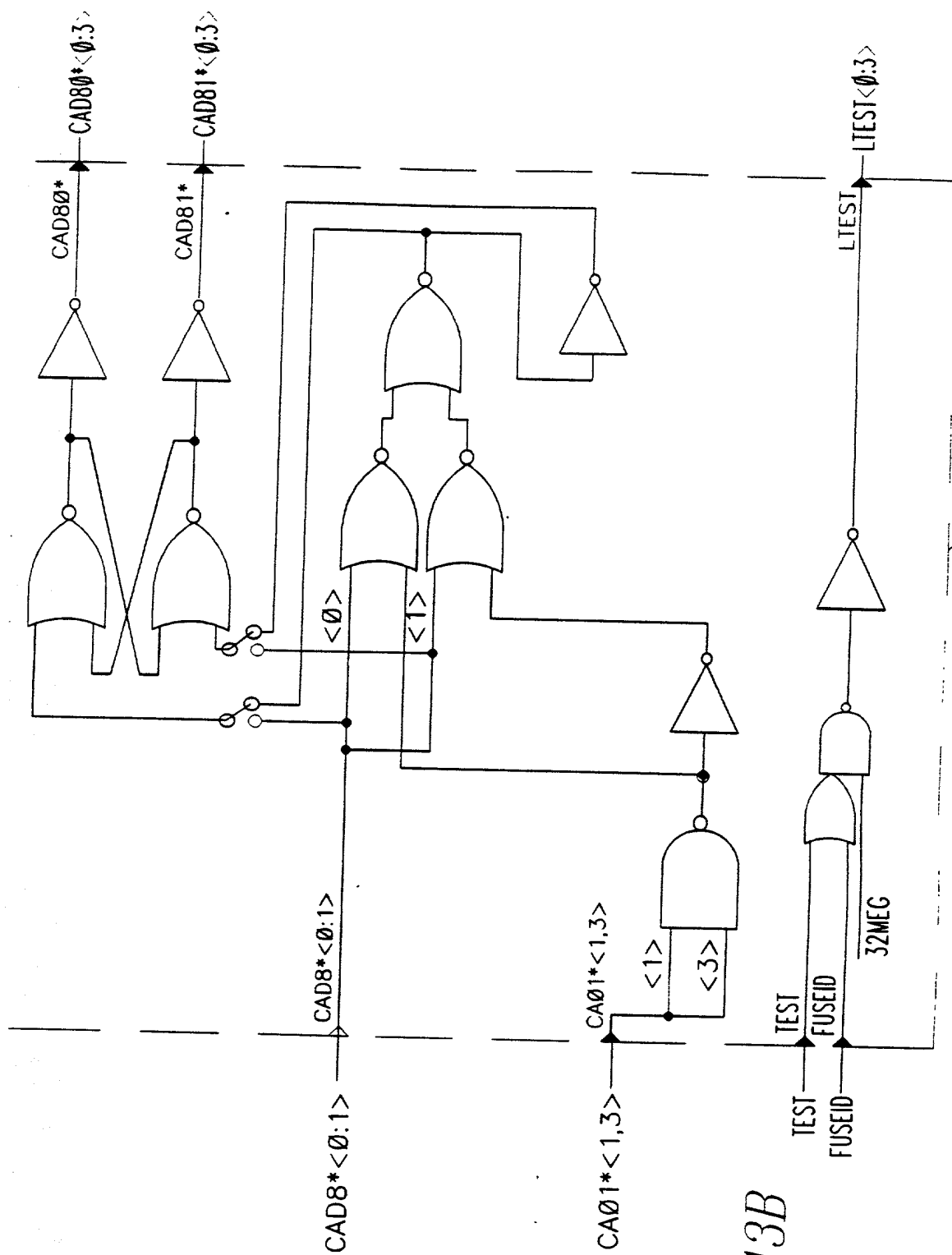


FIG. 13B

FIG. 11 is a schematic diagram of a logic circuit for a microprocessor system. The circuit includes a multiplexer (muxDecodeA 150) and a decoder (GOA4). The multiplexer has inputs labeled <0>, <1>, <2>, <3>, <4>, <5>, <6>, and <7>. The decoder has inputs labeled <0>, <1>, <2>, and <3>. The circuit also includes a 4K resistor, a 16MEG\* resistor, and a 4K resistor. The output of the circuit is labeled V1\* and V3\*.

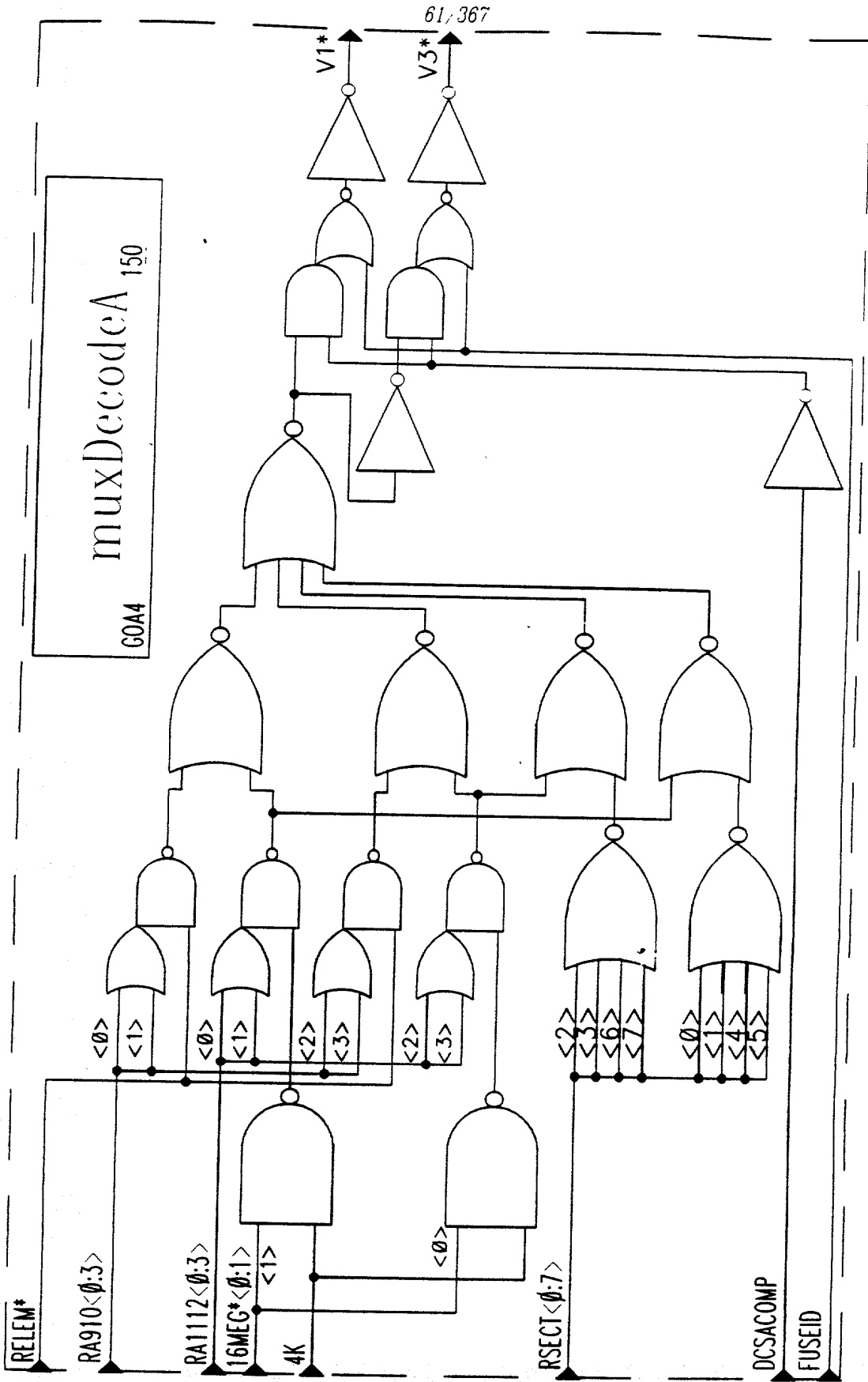


FIG. 11

FIG 15-1

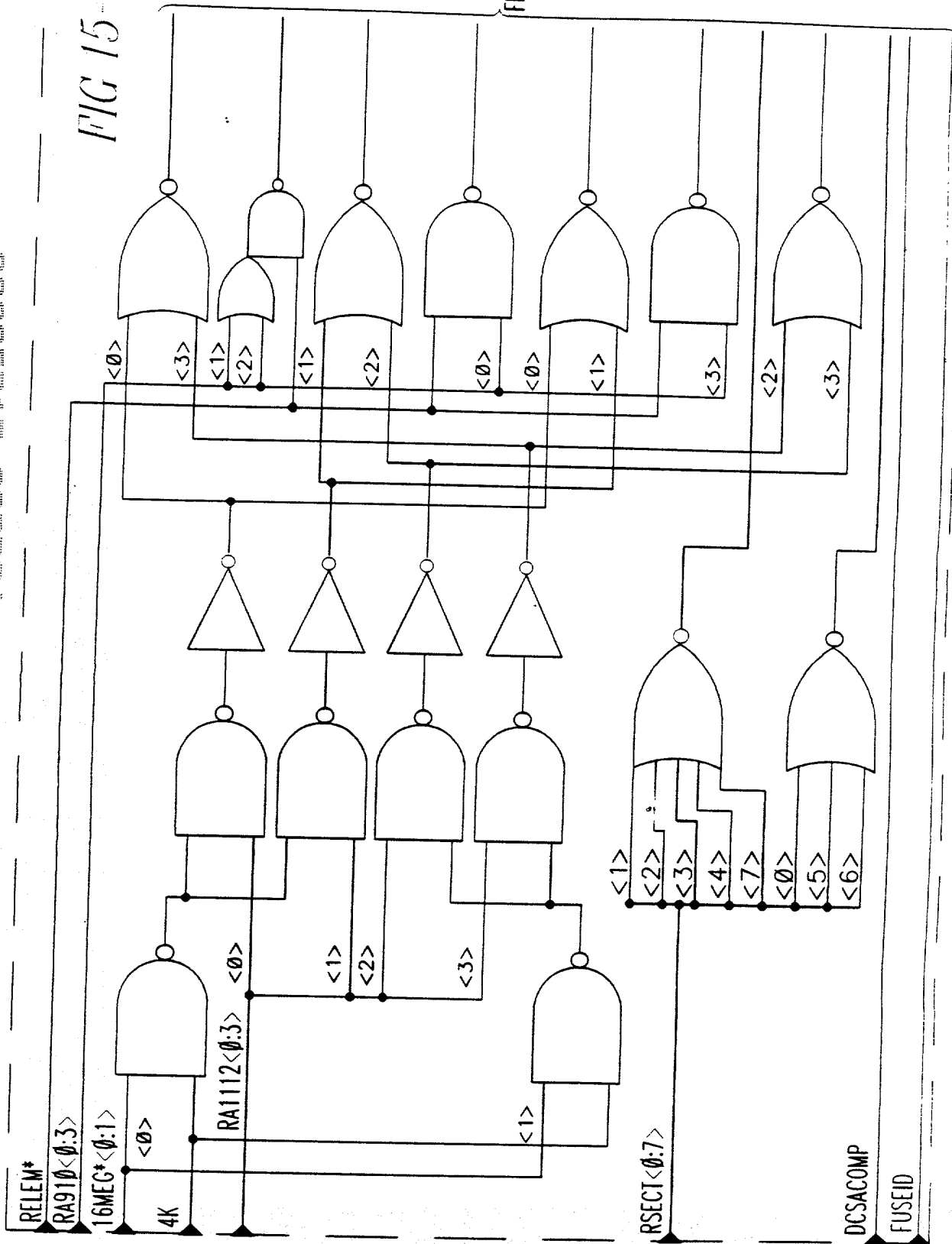
10  
FIG.15-2

FIG. 15-2

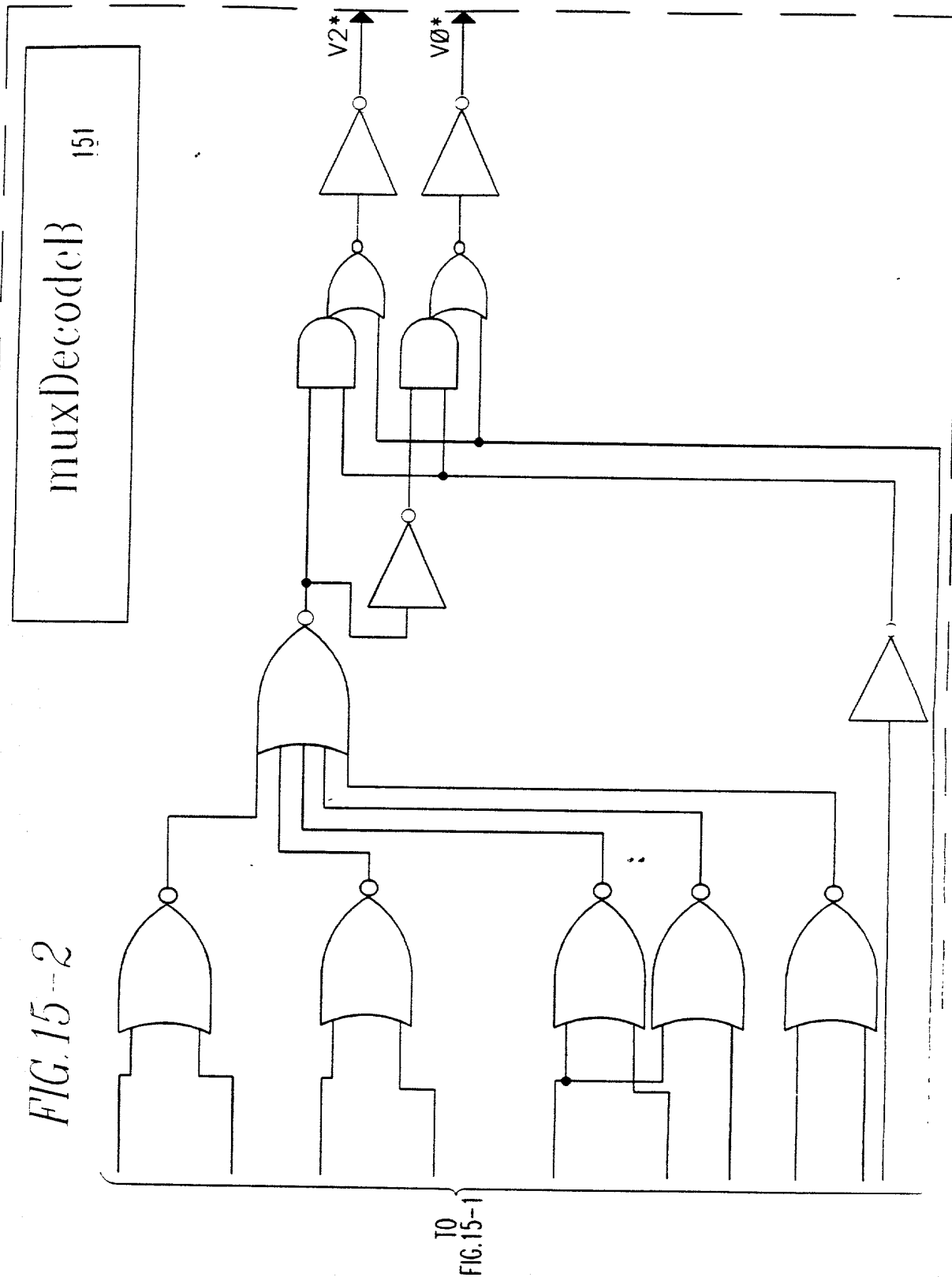
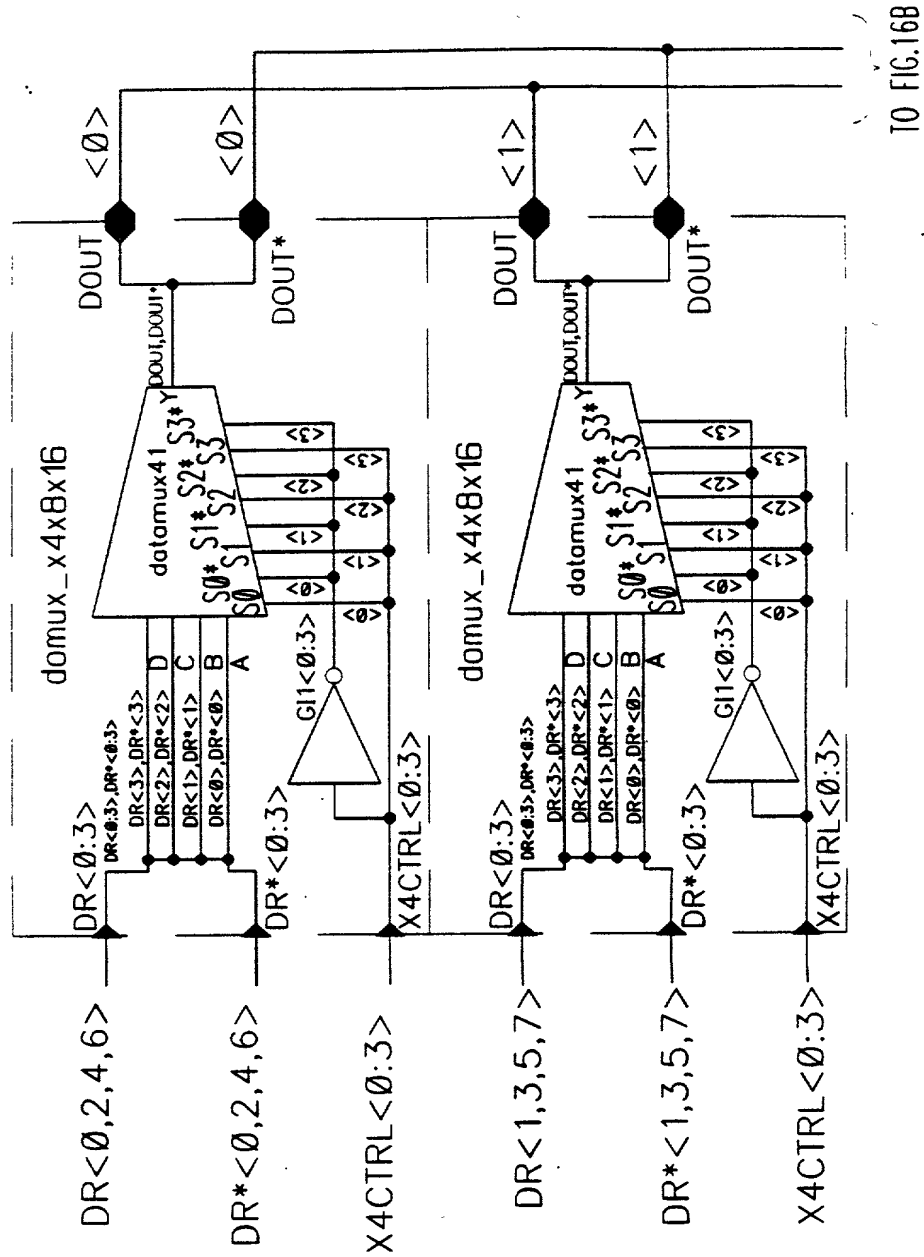
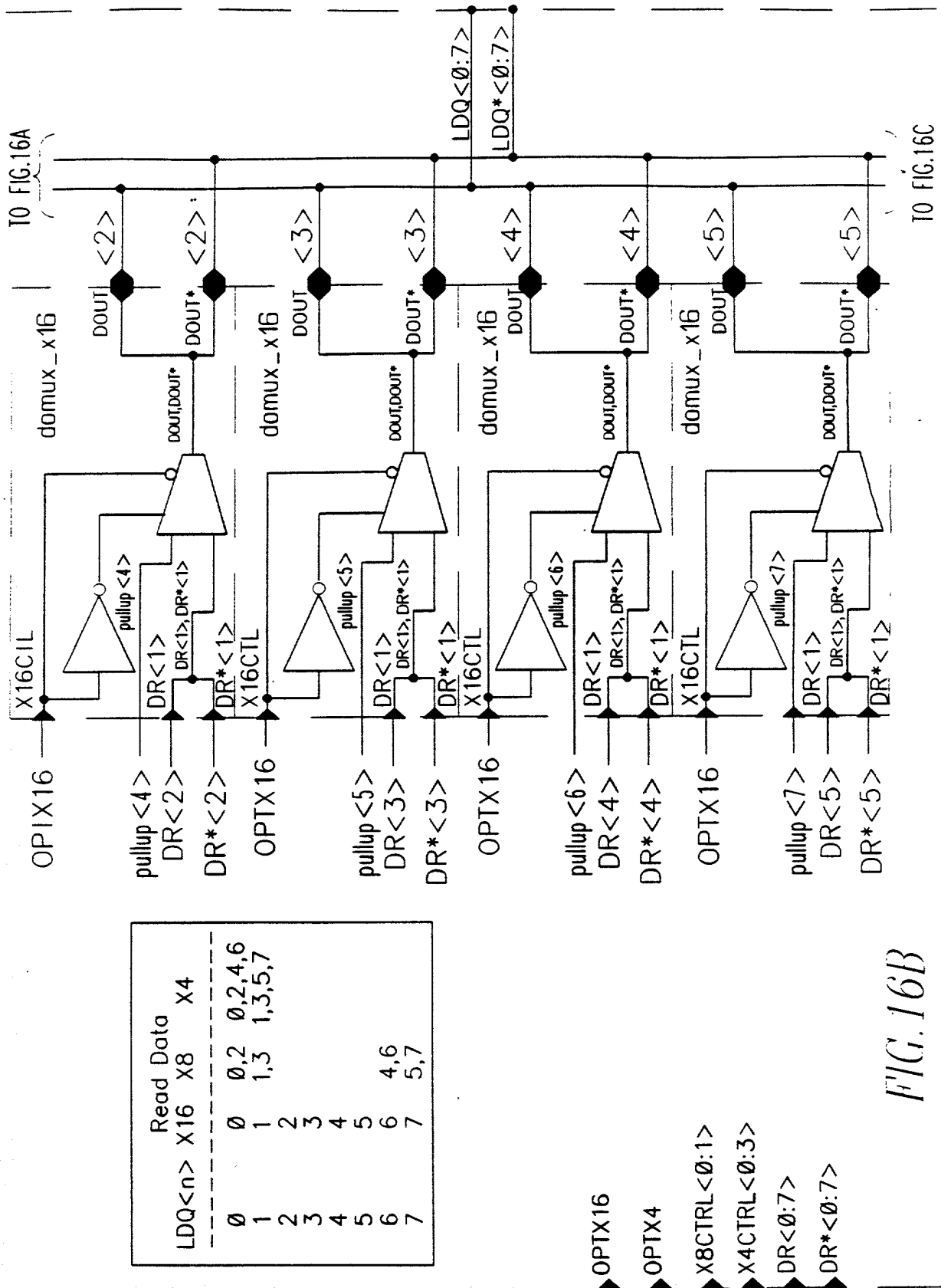


FIG. 16A







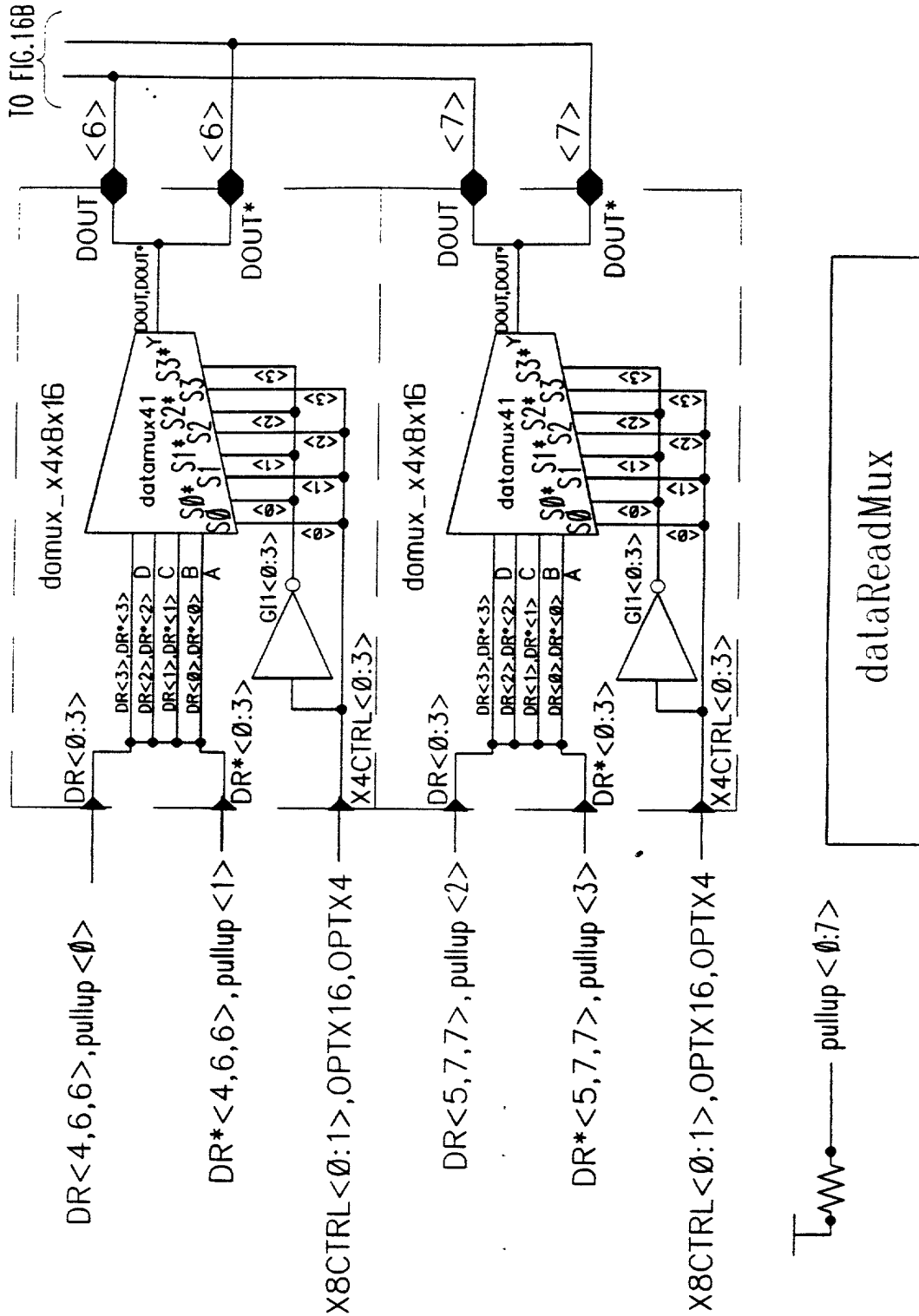


FIG. 26 is a schematic diagram of a data read multiplexer control circuit. The circuit includes a data read multiplexer (dataReadMux) and a data read multiplexer control circuit (dataReadMuxCtrl). The data read multiplexer has four data inputs (DQ<0:7>, DQ<8:15>, DQ<16:23>, DQ<24:31>) and one data output (DQ<0:31>). The data read multiplexer control circuit has four control inputs (CAI011\* <0:3>, OPTX4, OPTX8, OPTX16) and one control output (OPTX16). The control circuit is implemented using a series of logic gates (AND, OR, NOT) and inverters. The control circuit generates control signals (X4CTRL <0:3>, X8CTRL <0:1>) that are used to select the data input for the data read multiplexer. The control circuit also generates control signals (LDQ\* <0:7>, LDQ <0:7>) that are used to enable the data read multiplexer. The control circuit is shown in FIG. 17 and FIG. 18.

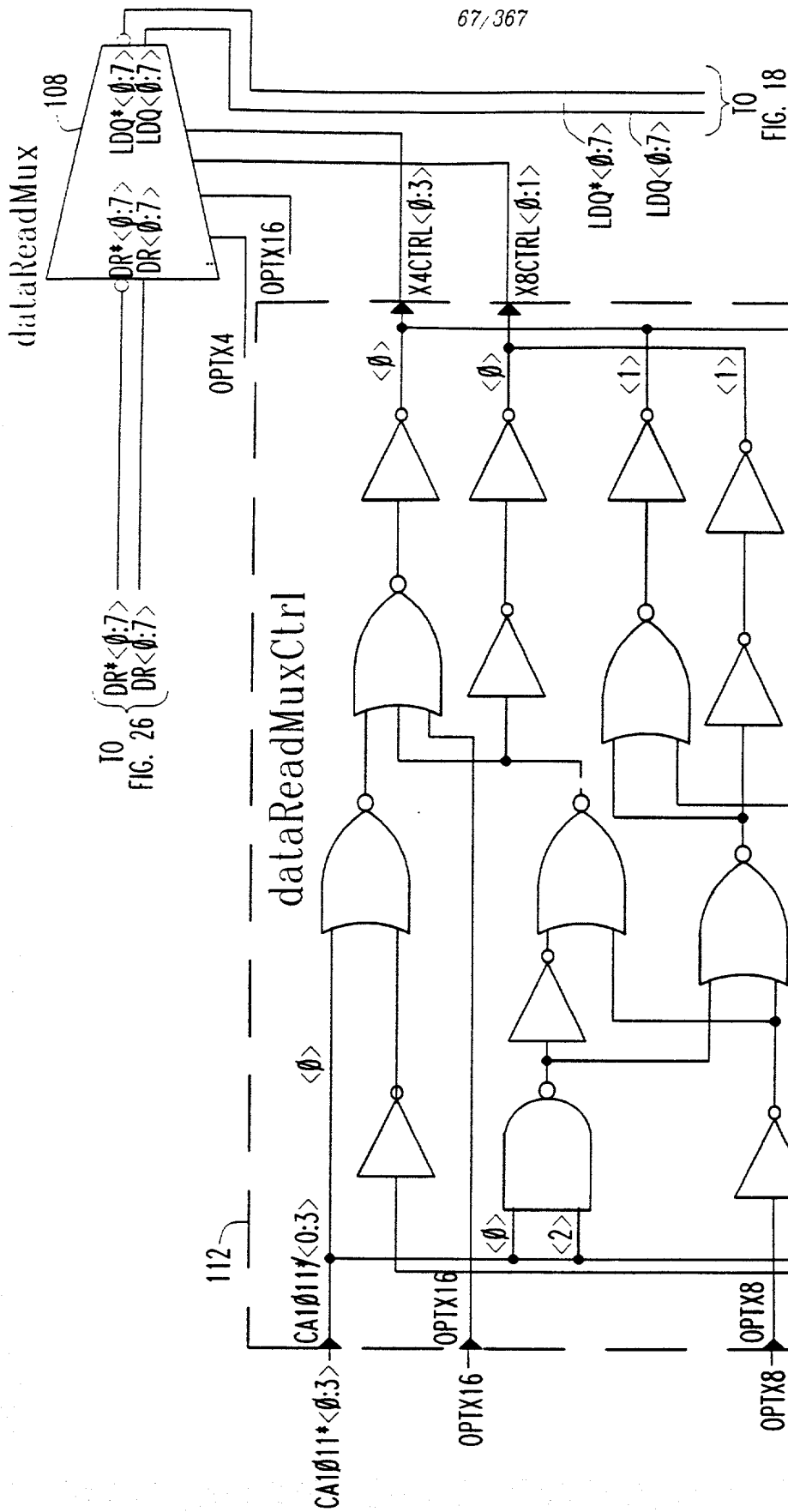
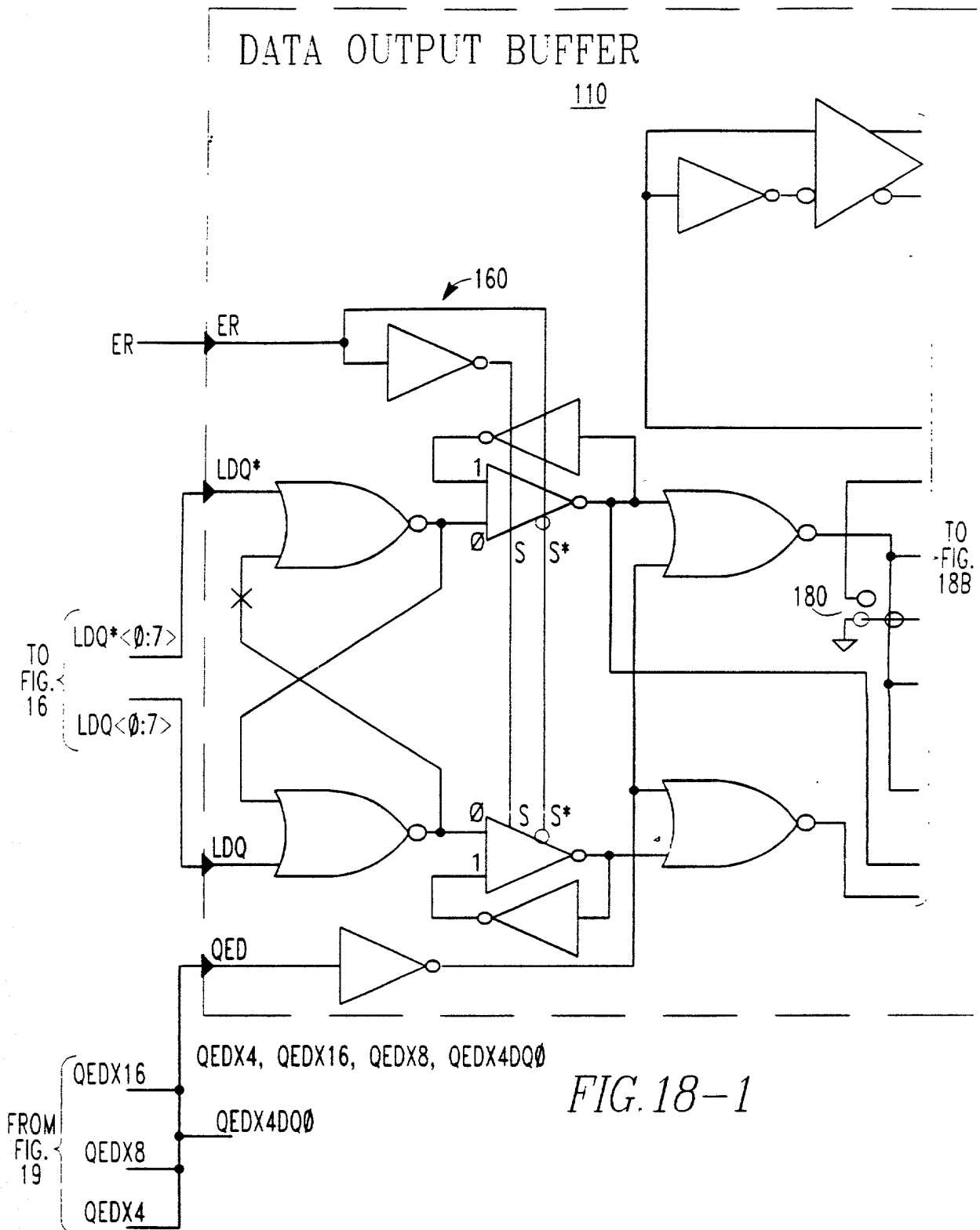


FIG. 17

FIG. 18



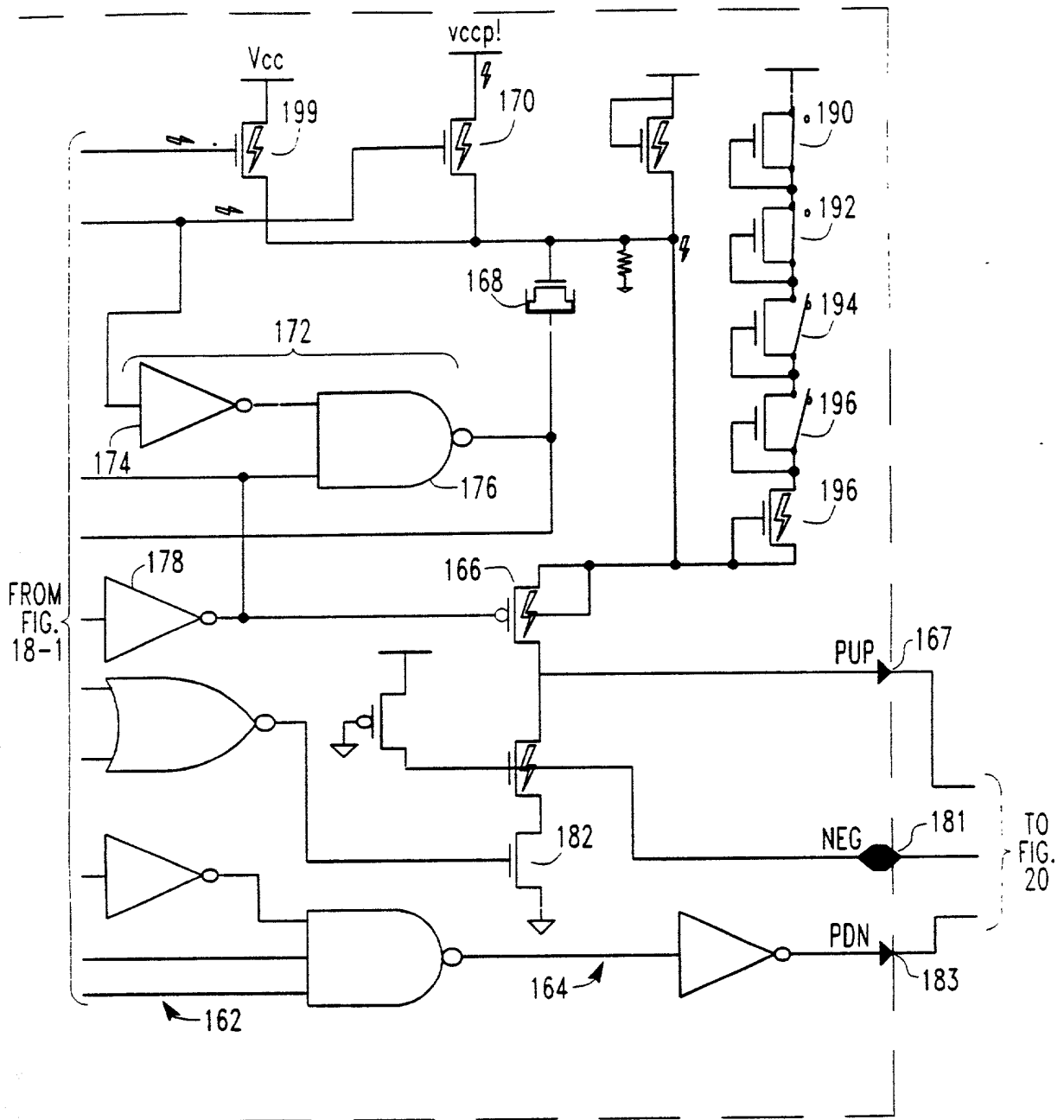


FIG. 18-2

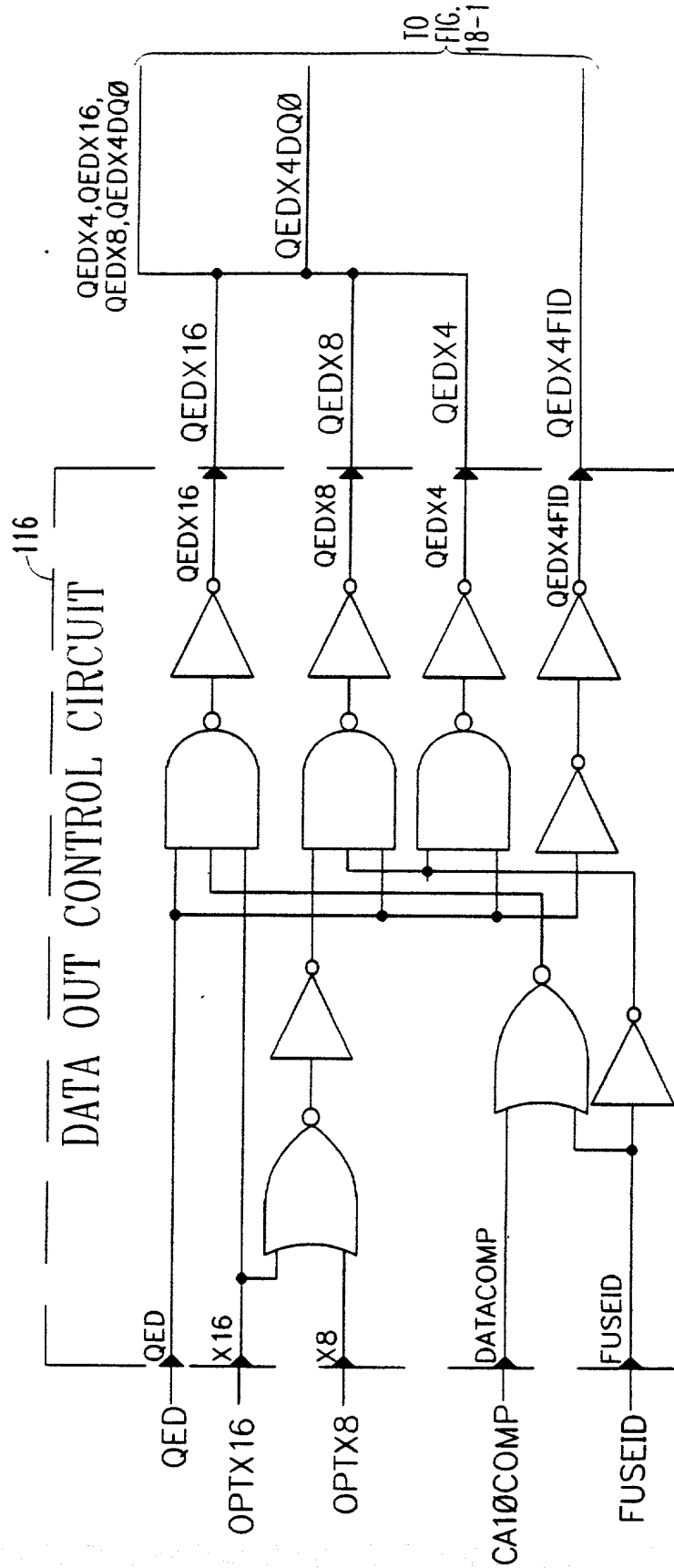


FIG. 19

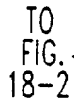


FIG. 20

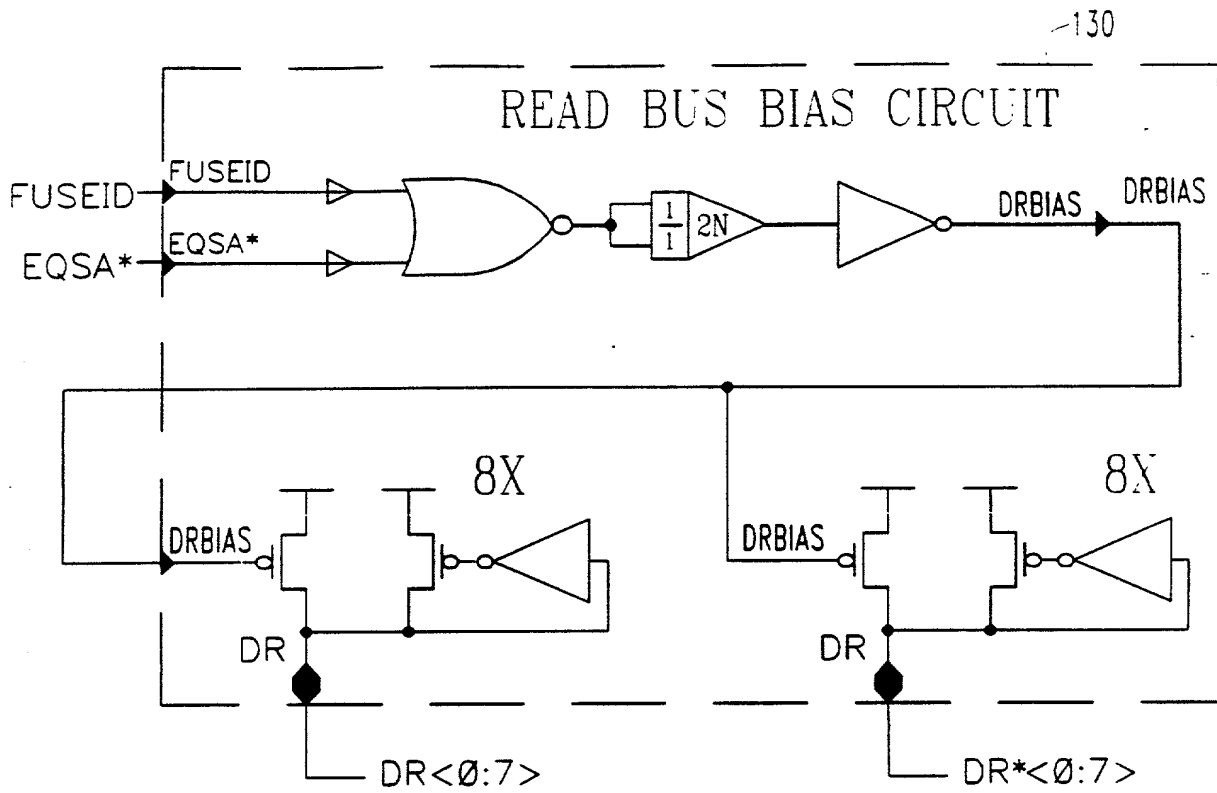


FIG. 21



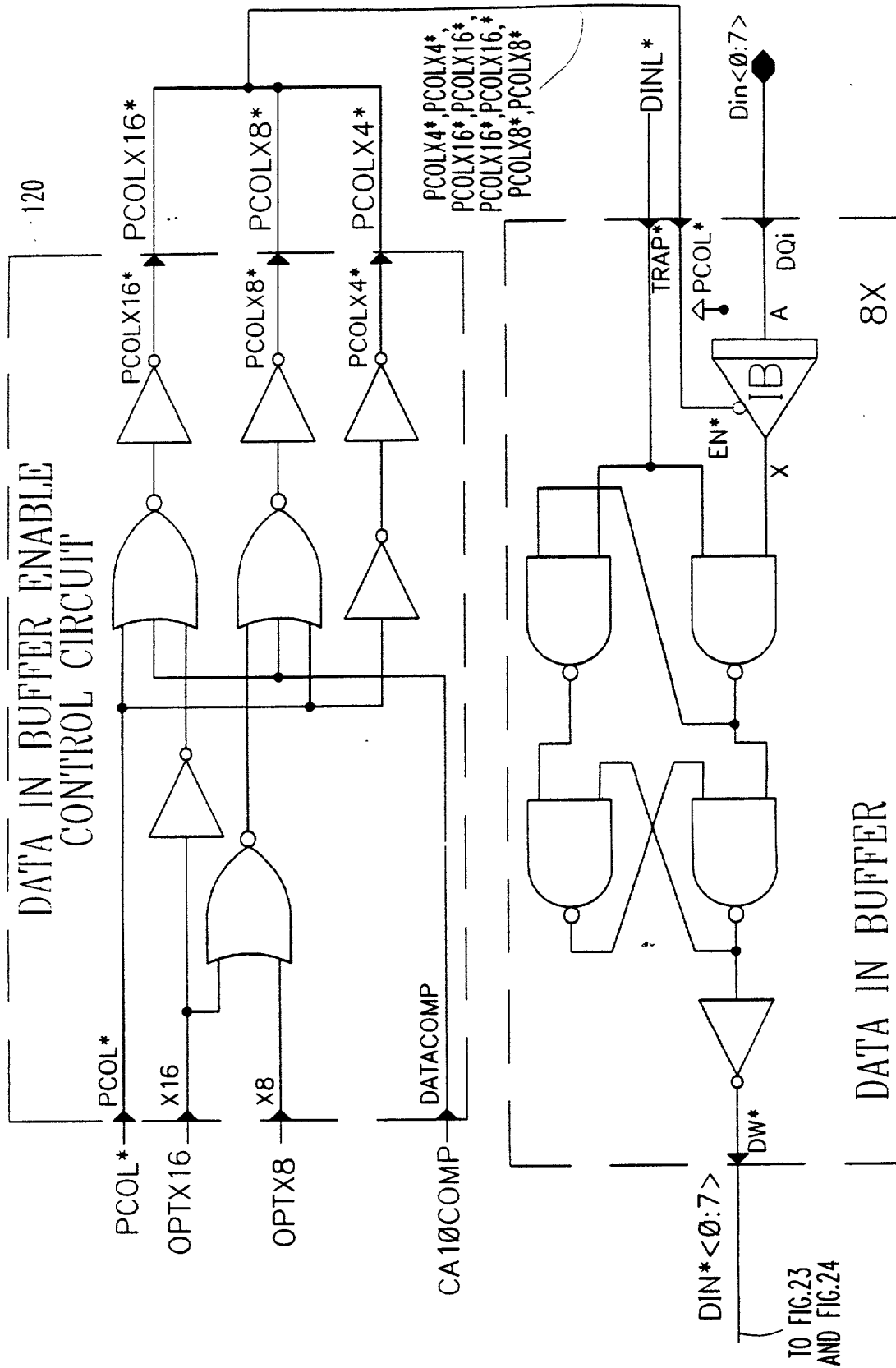
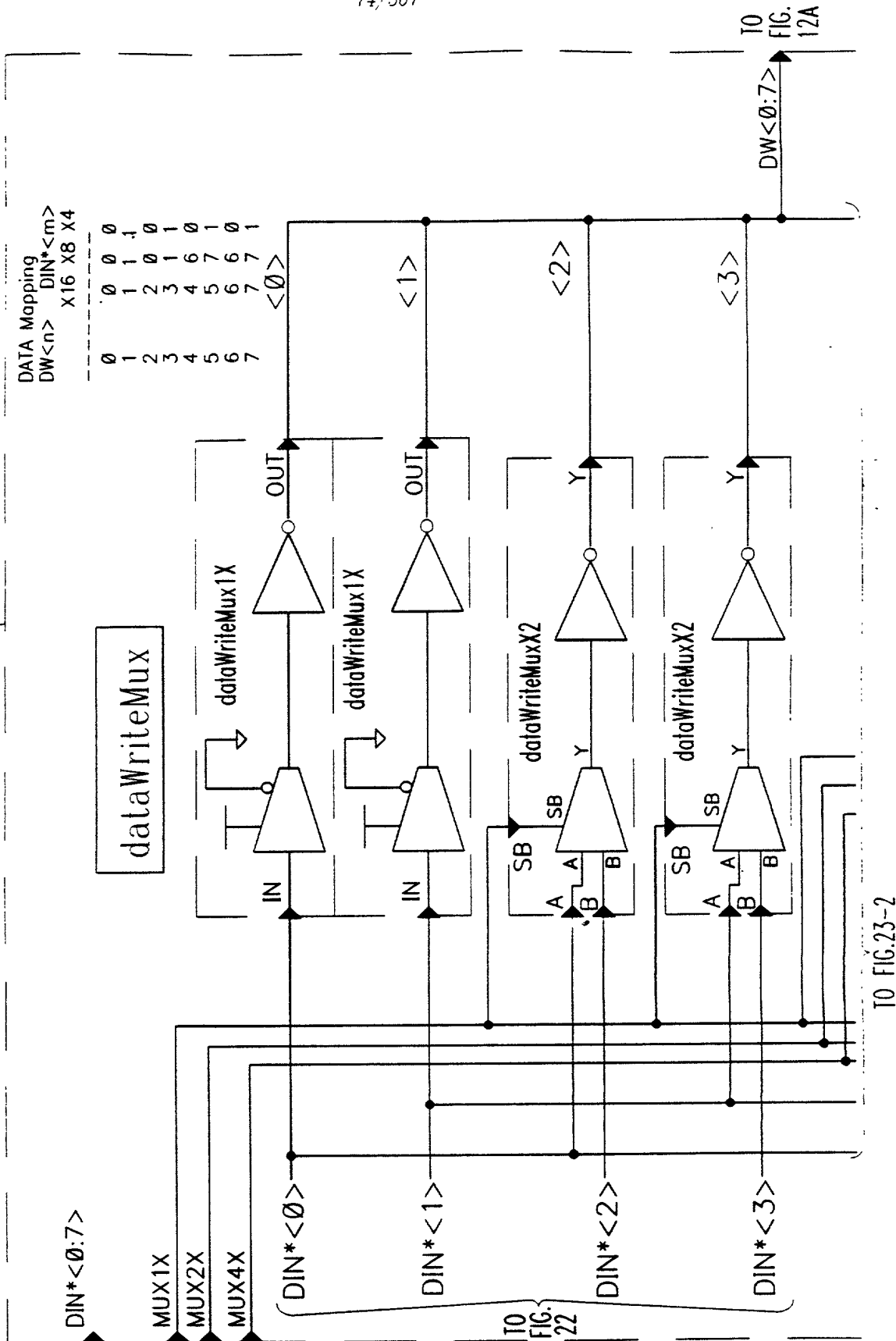
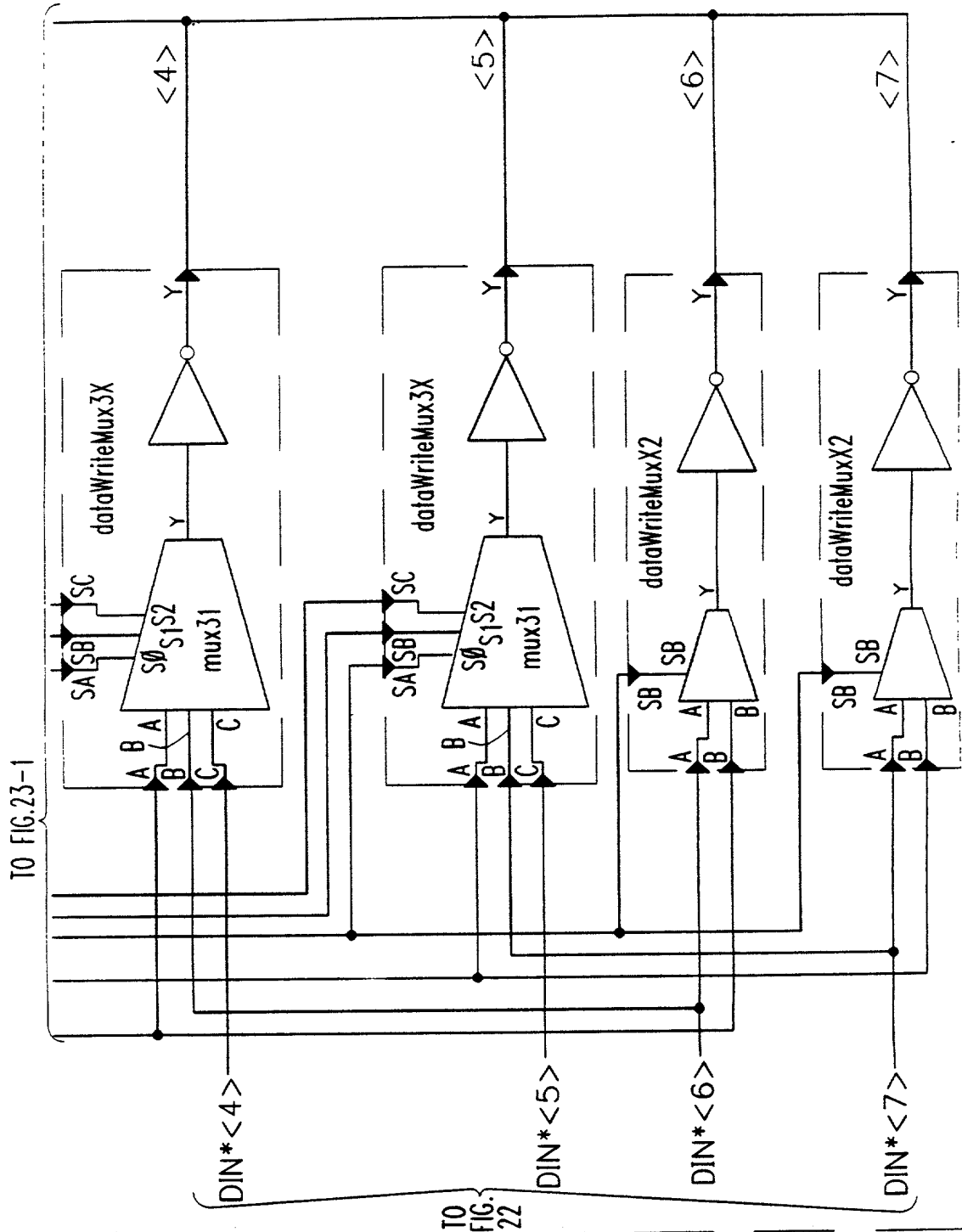


FIG. 23-1



TO FIG. 23-2



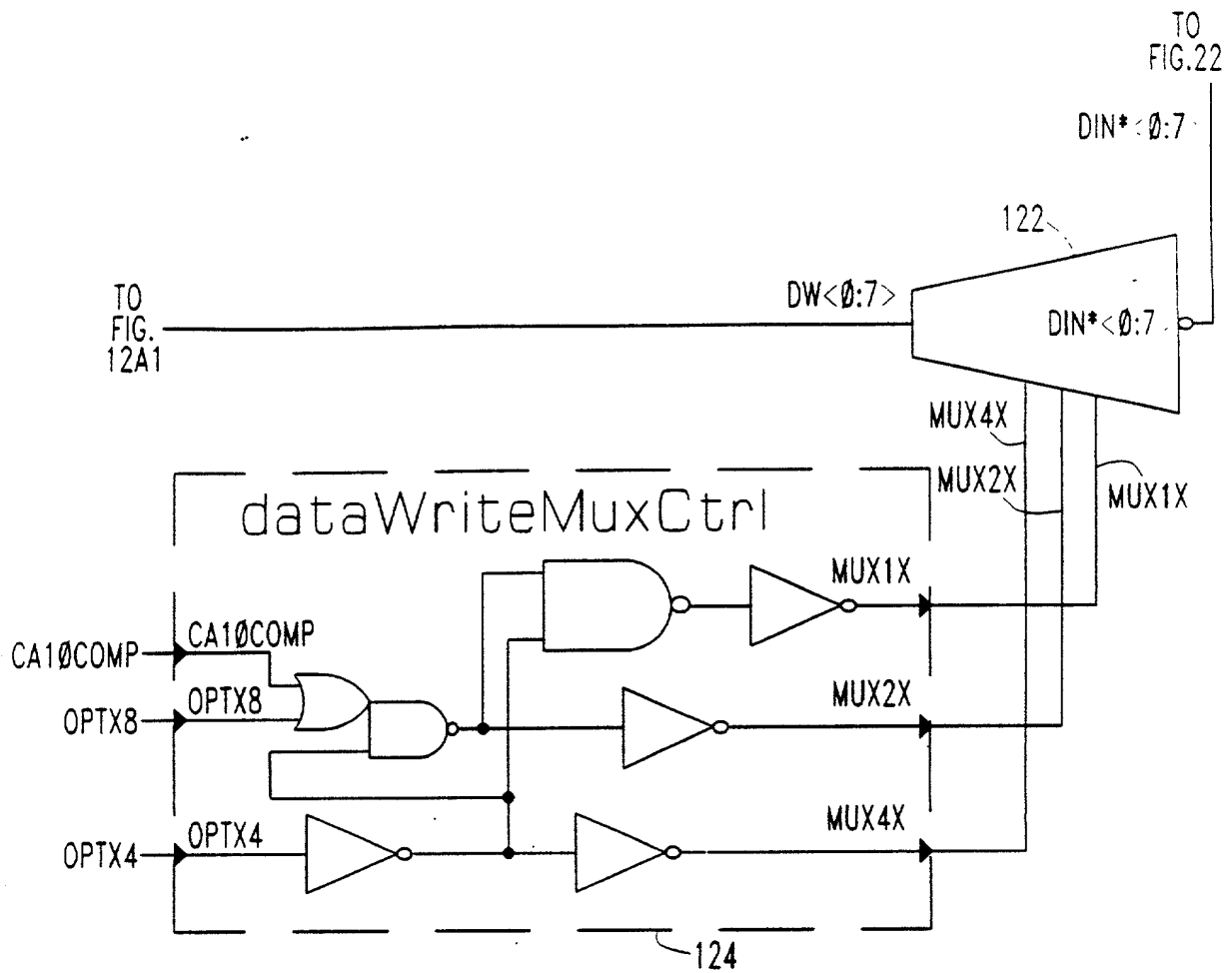


FIG. 24

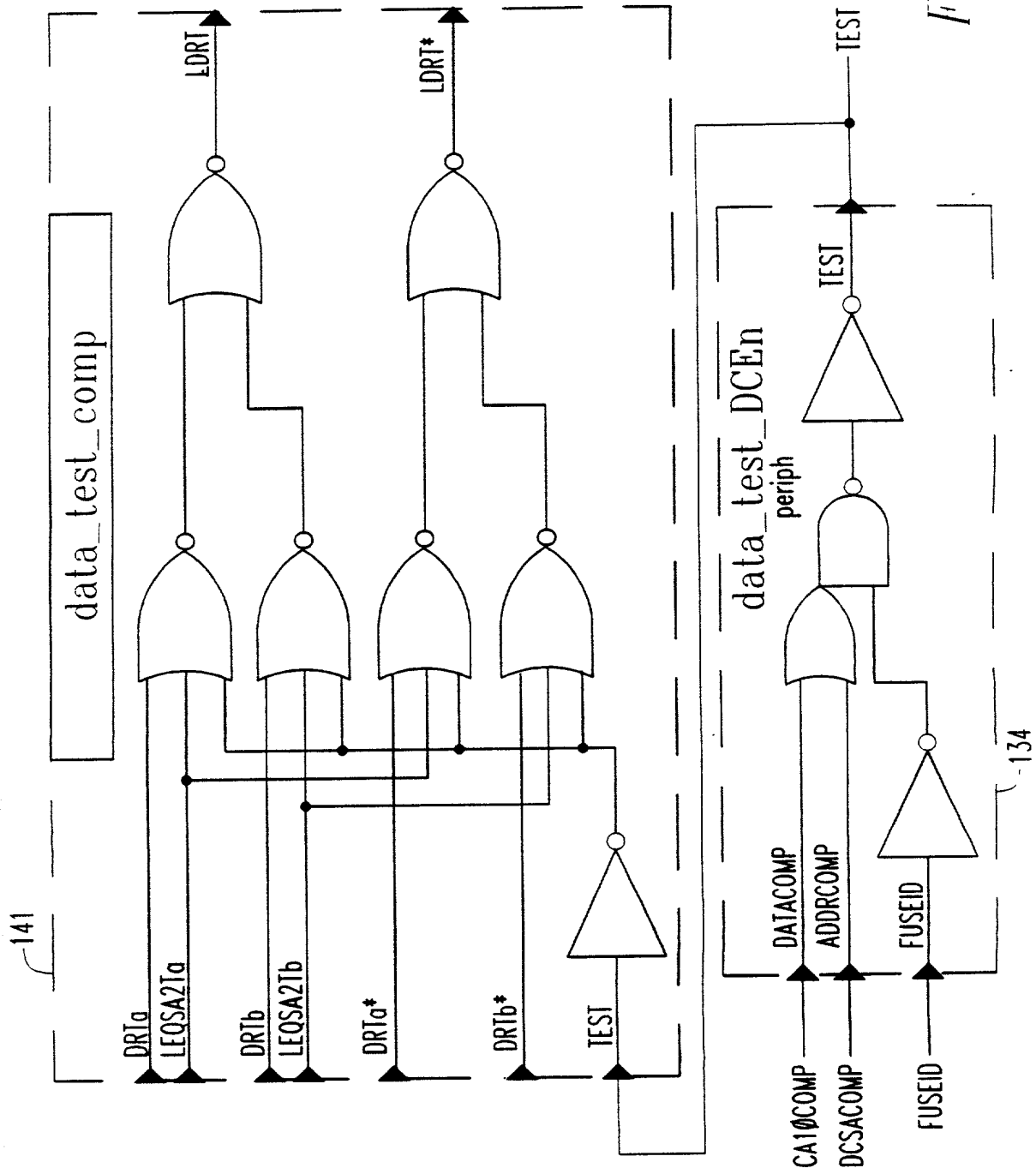


FIG. 25

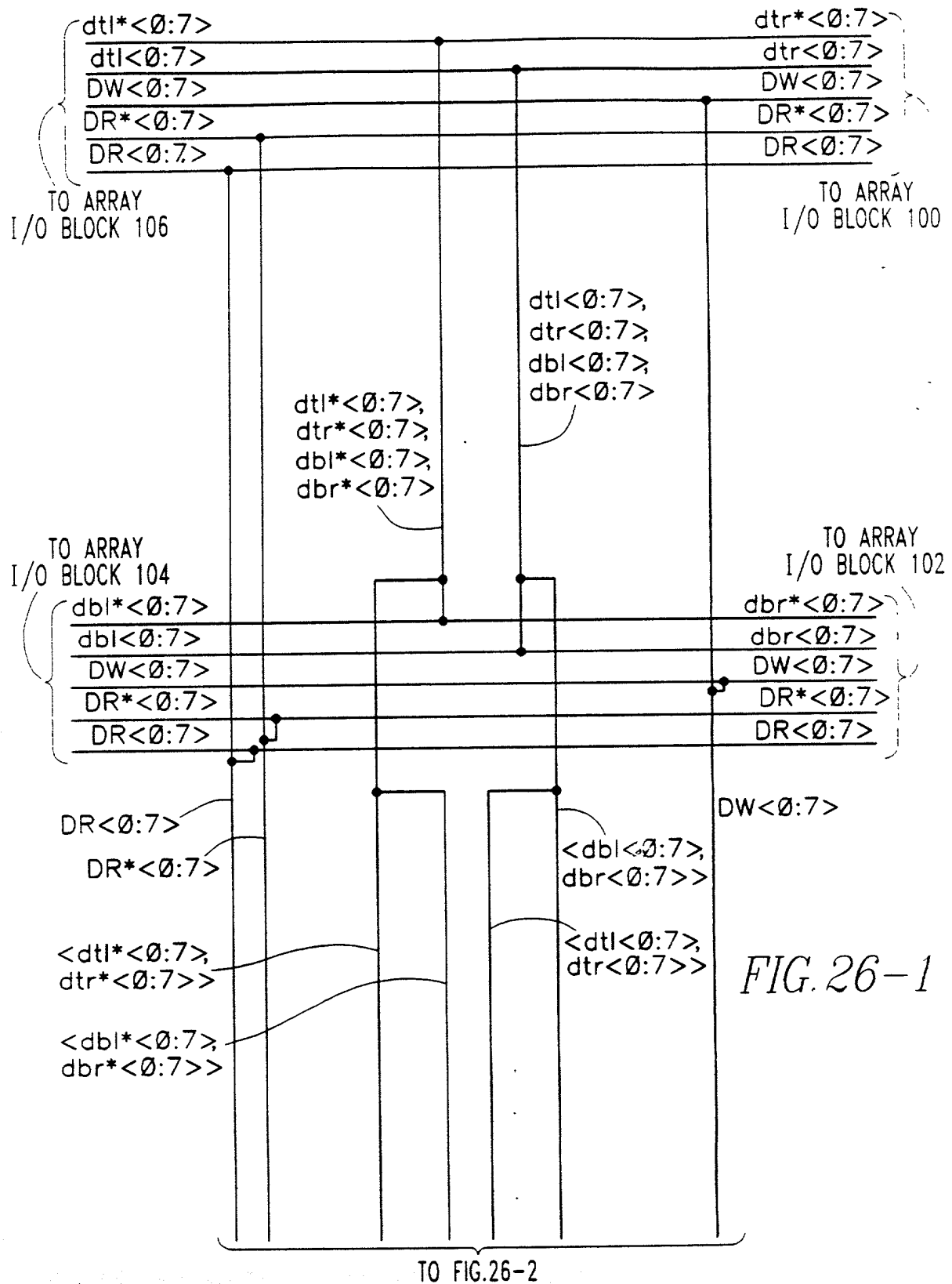


FIG. 26-1

FROM FIG.26-1

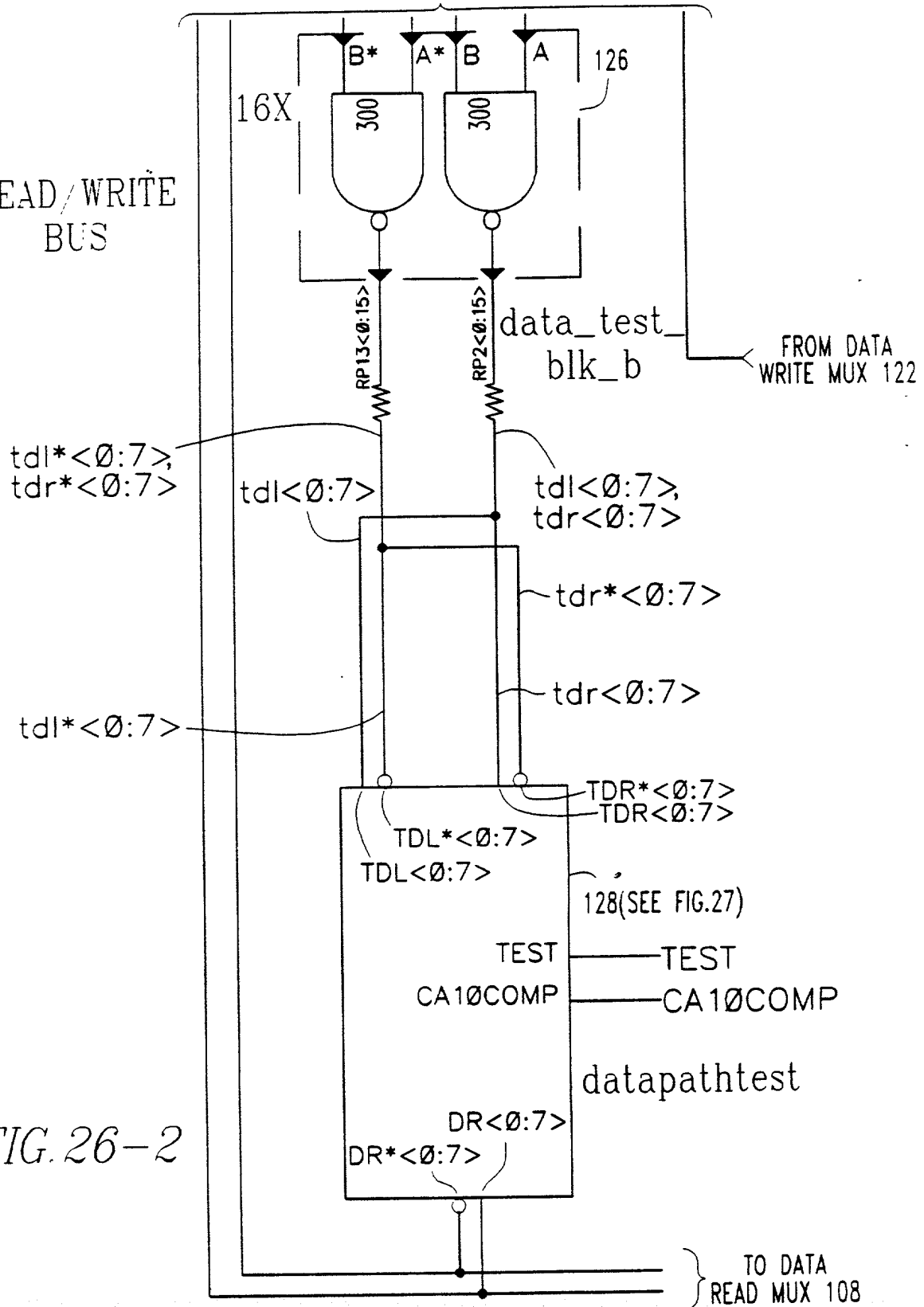
READ/WRITE  
BUS

FIG.26-2

80/367

TO  
FIG.  
27-2

CA10COMP

TEST

TDL<0:7>

TDL\*<0:7>

<0>

<0>

<1>

<2>

<2>

<3>

<3>

<4>

<4>

<5>

<5>

<6>

<6>

<7>

<7>

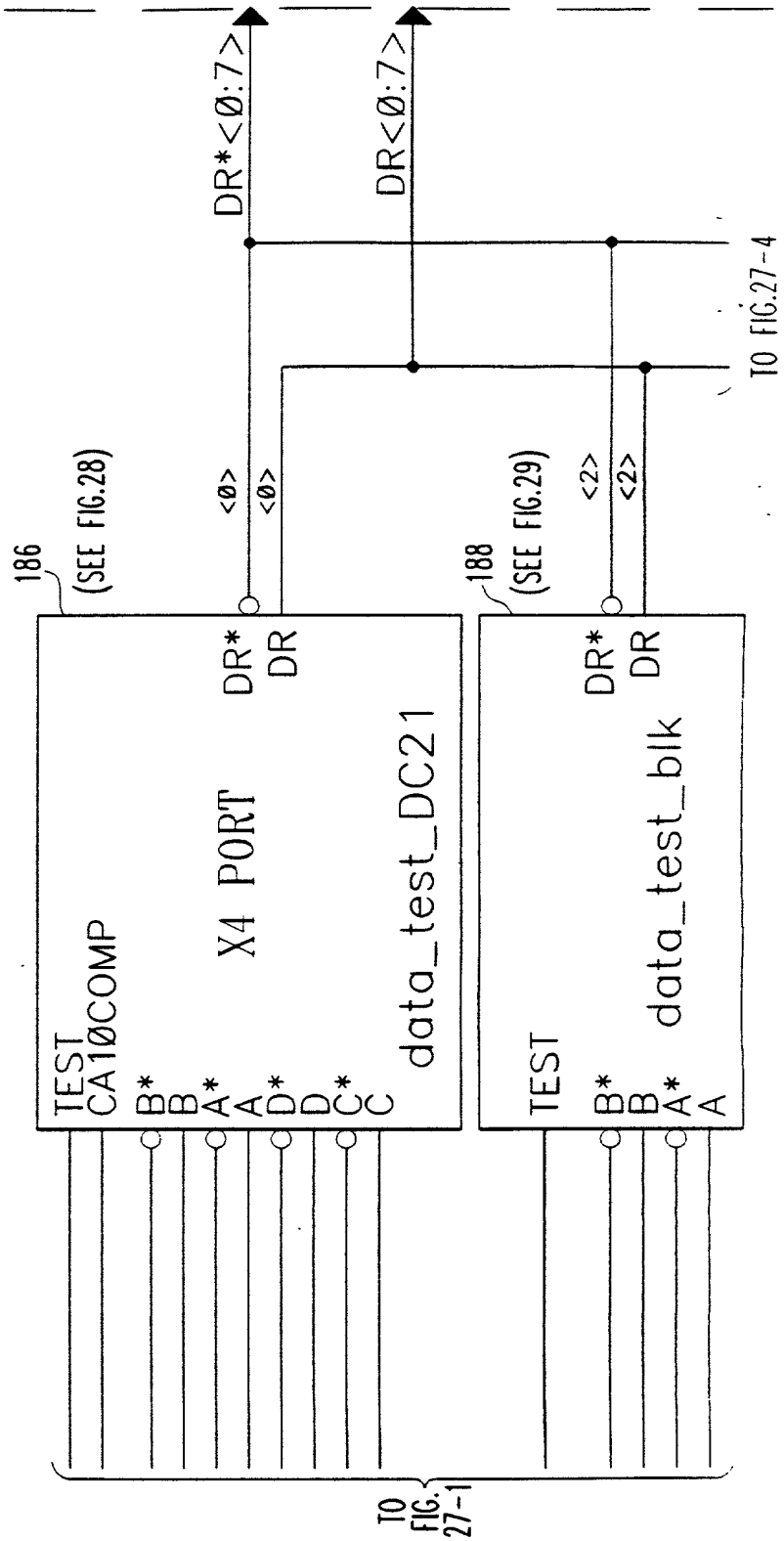
TO FIG.27-3

FIG.27-1



FIG. 27 2

dataPathTest  
Block 128



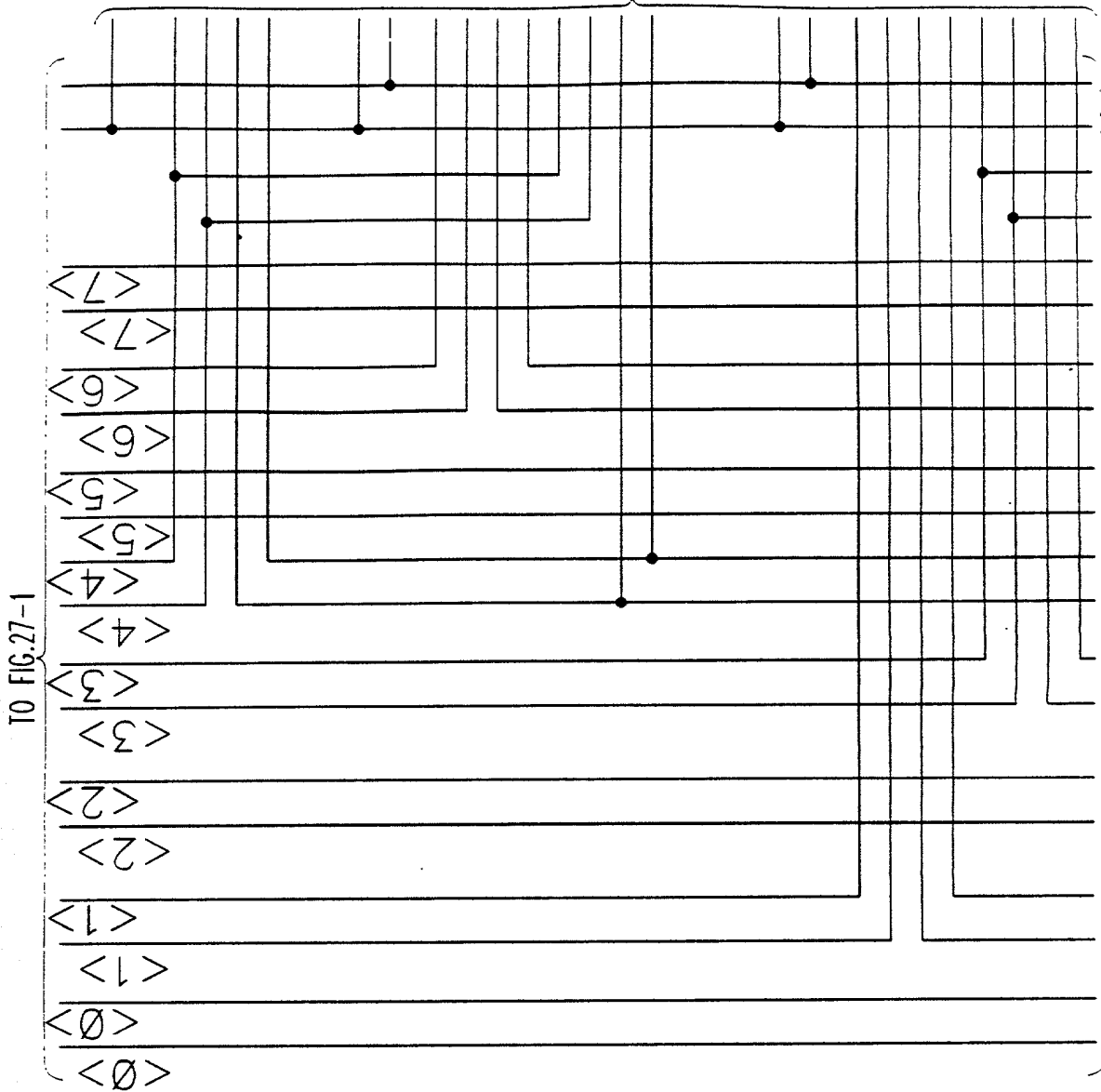
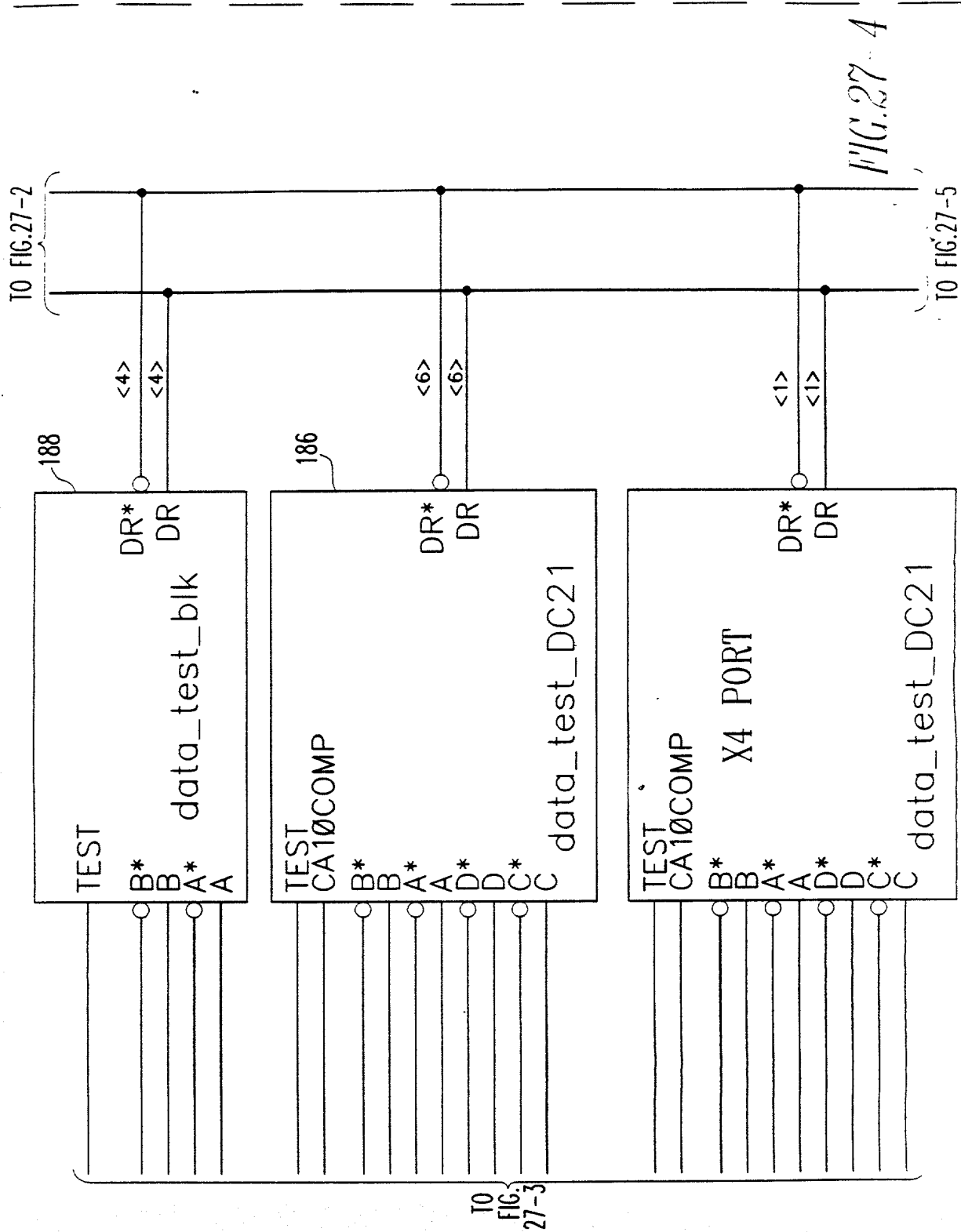


FIG. 27-3



10 FIG.27-3

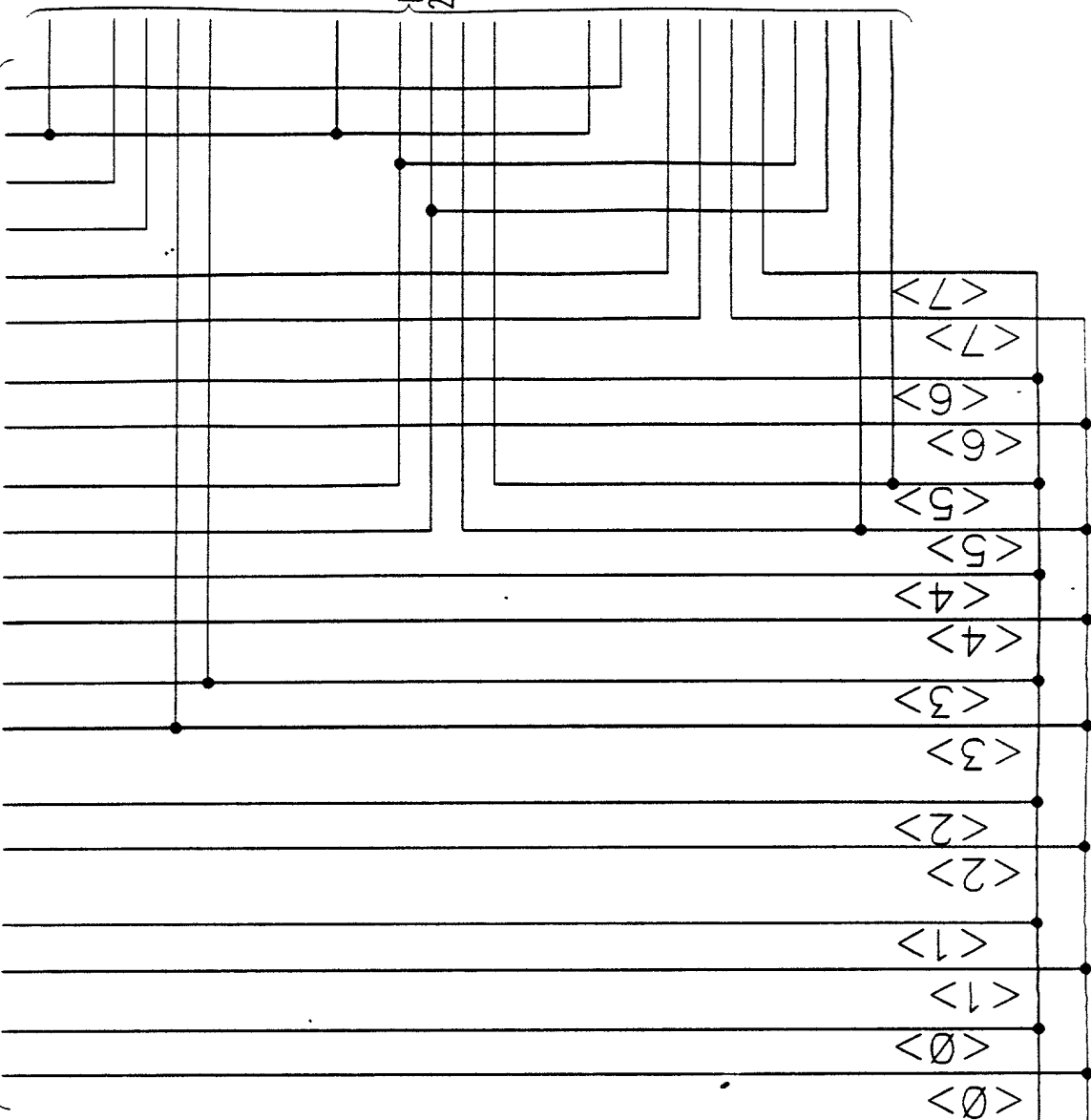
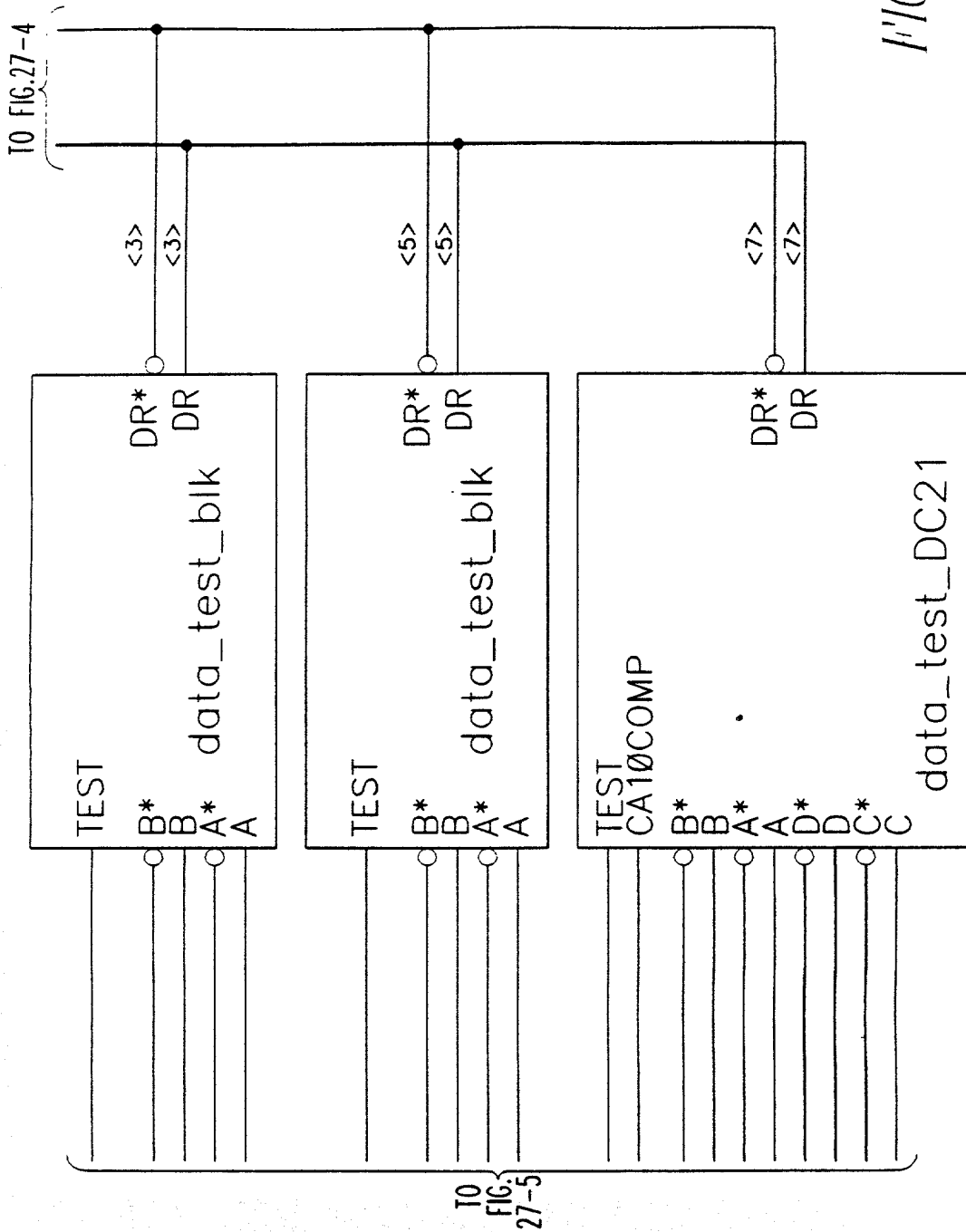


FIG.27-5

TDR<0:7>  
TDR\*<0:7>



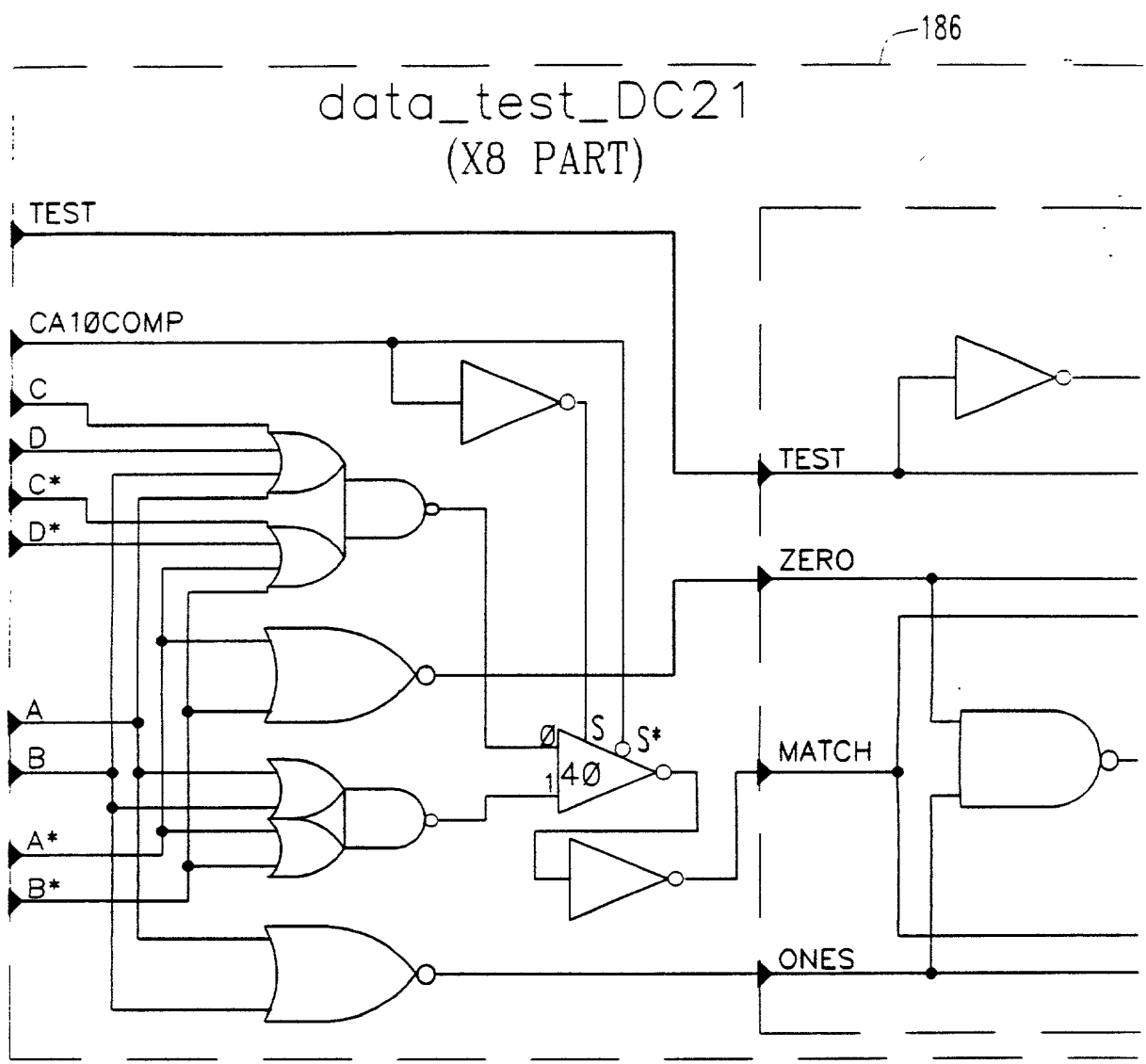


FIG. 28-1

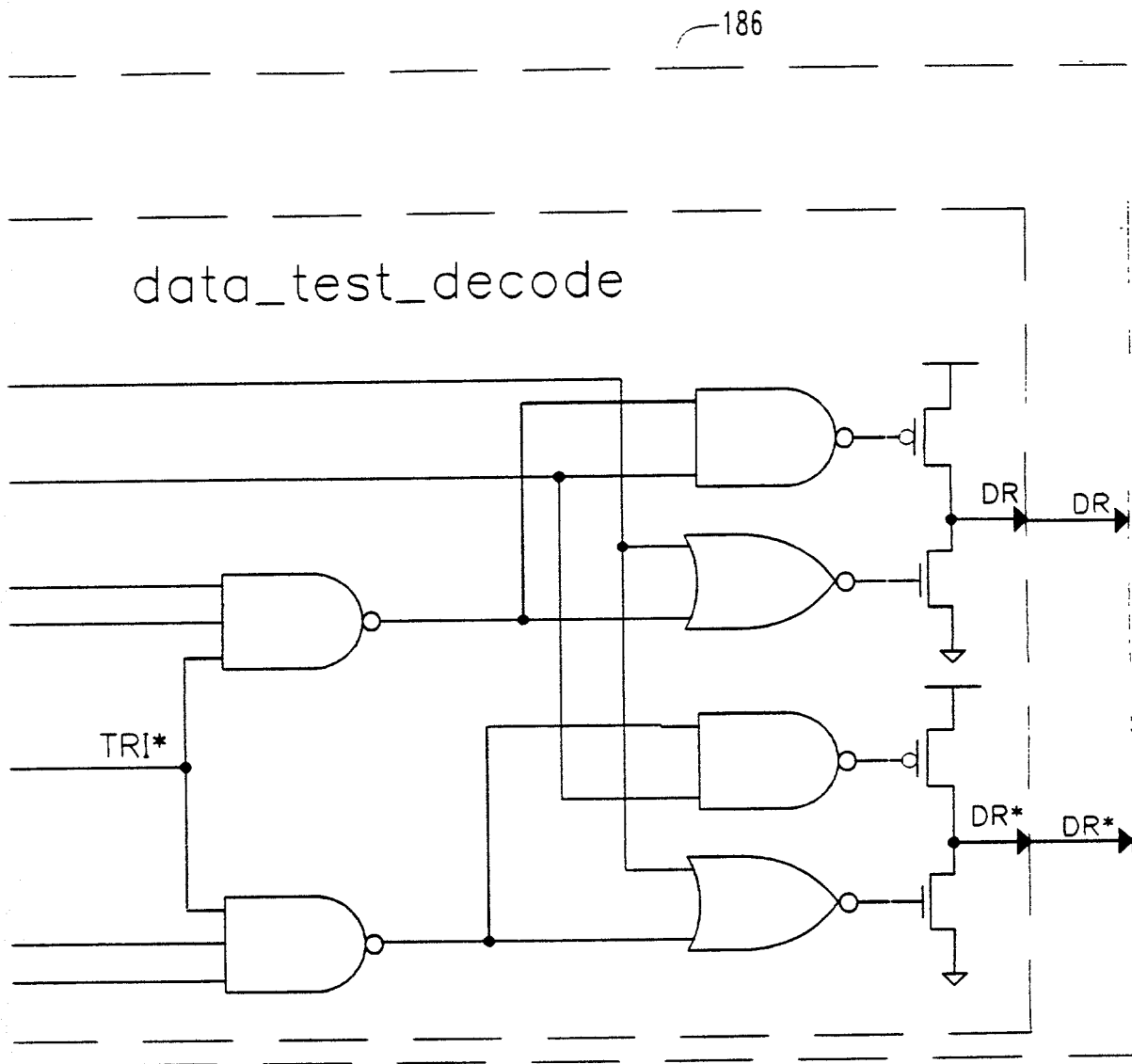


FIG. 28-2

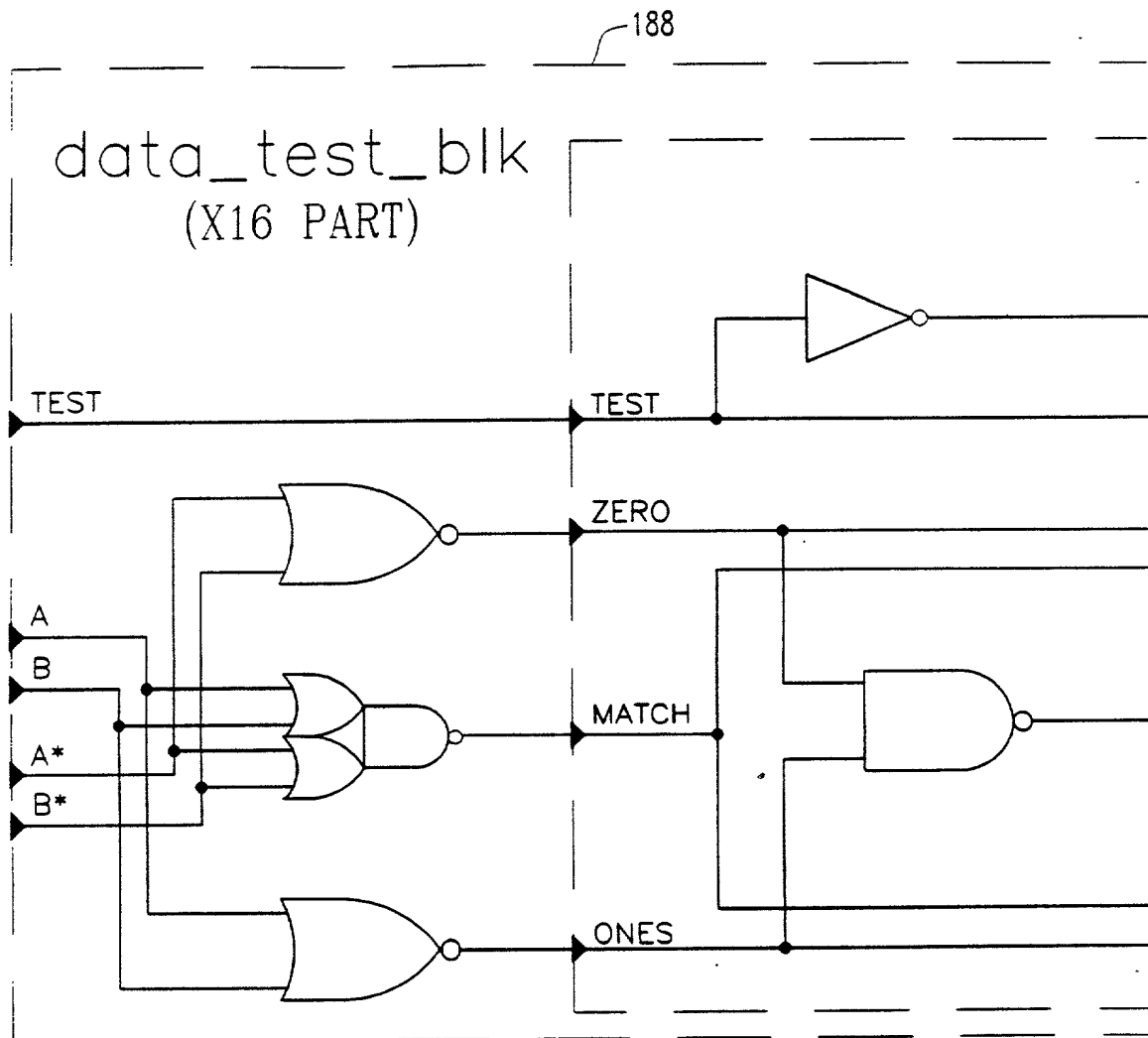


FIG. 29-1



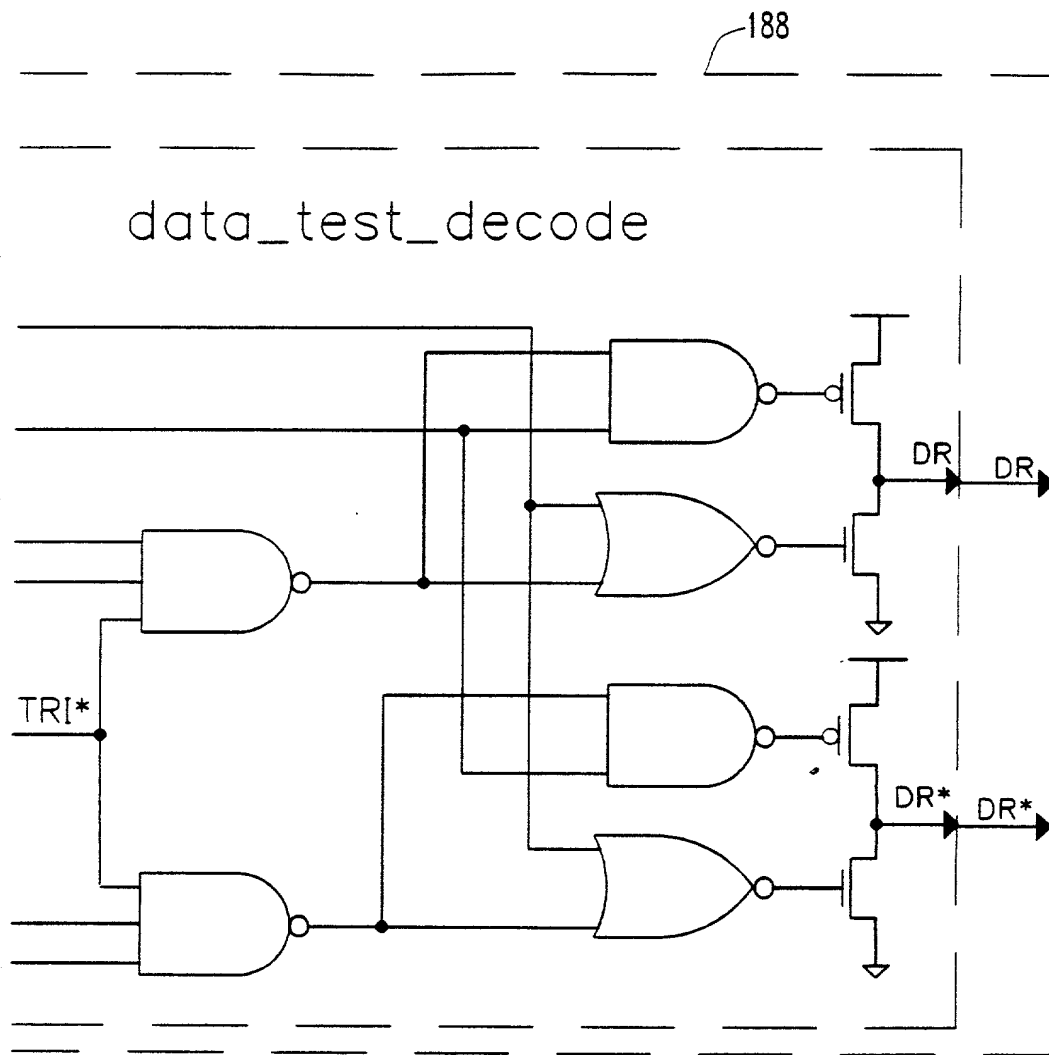
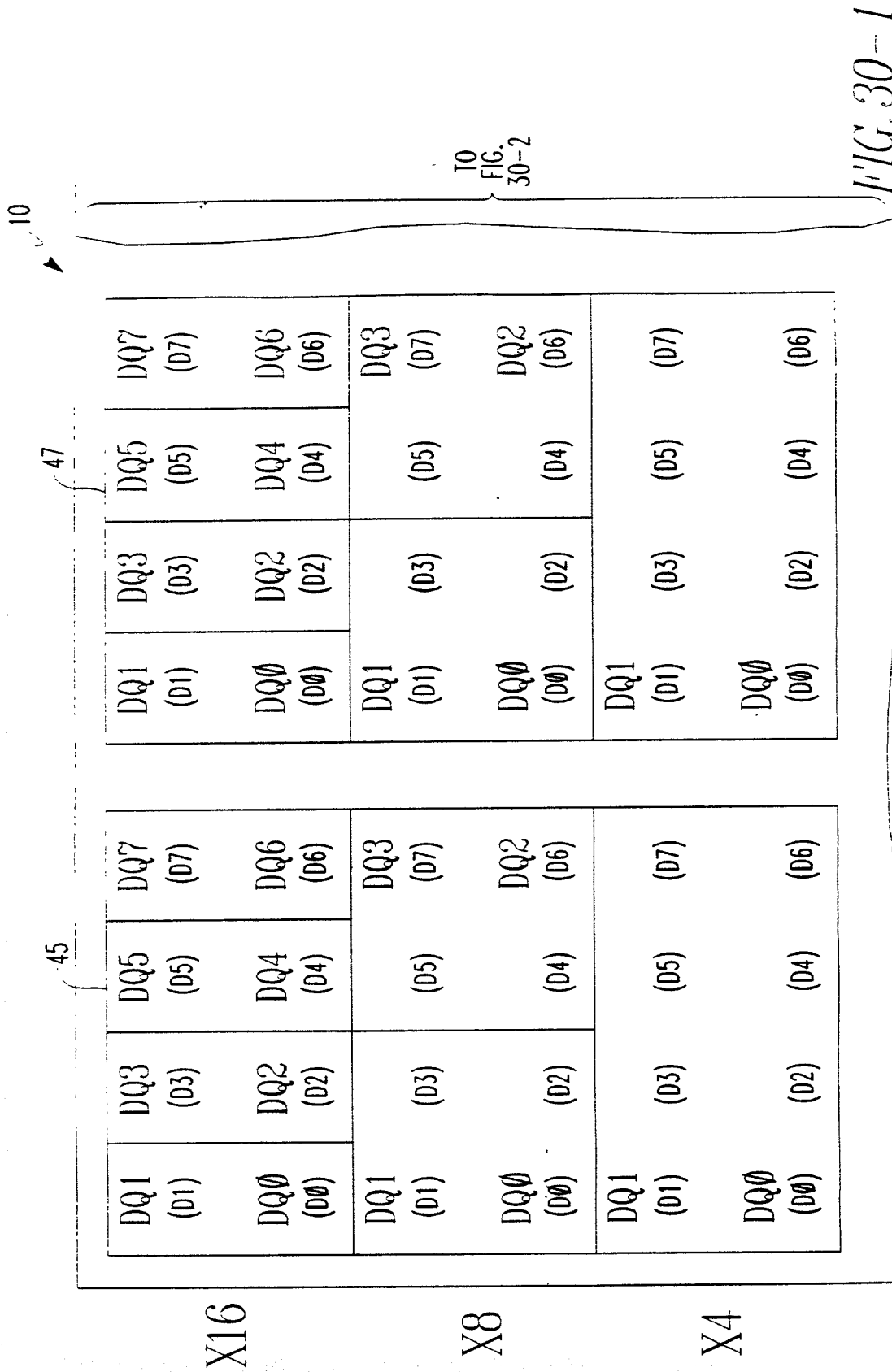
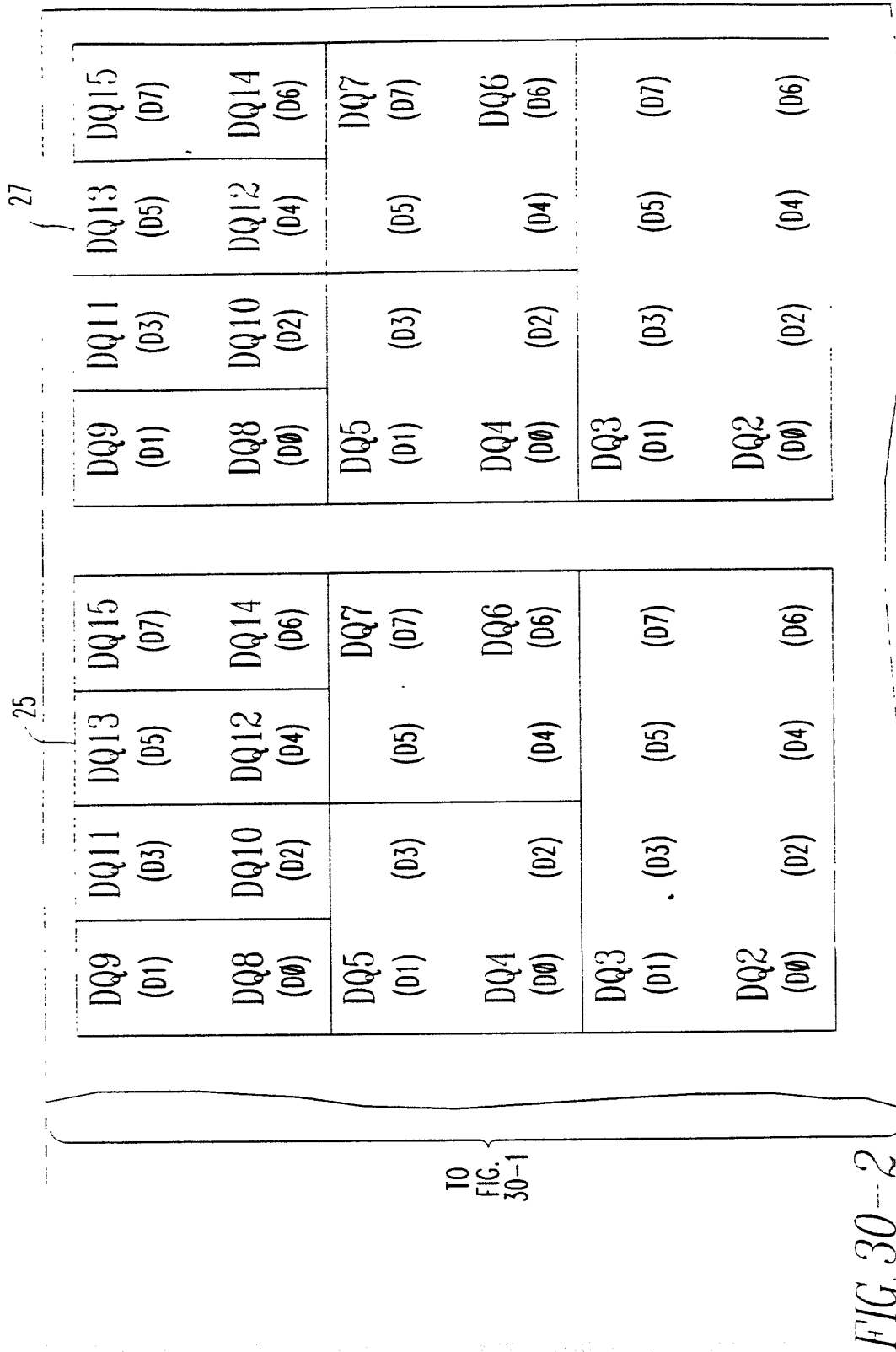


FIG. 29-2



TO FIG. 30-3



10 FIG. 30-4

TO FIG. 30-1

	38				40			
	(00) DQ0	(02) DQ2	(04) DQ4	(06) DQ6	(01) DQ1	(03) DQ3	(05) DQ5	(07) DQ7
X4	(00) DQ0	(02) DQ2	(04) DQ4	(06) DQ6	(01) DQ1	(03) DQ3	(05) DQ5	(07) DQ7
X8	(00) DQ0	(02) DQ2	(04) DQ4	(06) DQ6	(01) DQ1	(03) DQ3	(05) DQ5	(07) DQ7
X16	(00) DQ0	(02) DQ2	(04) DQ4	(06) DQ6	(01) DQ1	(03) DQ3	(05) DQ5	(07) DQ7

TO  
FIG.  
30-4

FIG. 30 3

TO FIG. 30-2

31			(00) DQ2	(02)	(04)	(06)
			(01) DQ3	(03)	(05)	(07)
33			(00) DQ4	(02)	(04)	(06) DQ6
			(01) DQ5	(03)	(05)	(07) DQ7
			(00) DQ8	(02) DQ10	(04) DQ12	(06) DQ14
			(01) DQ9	(03) DQ11	(05) DQ13	(07) DQ15

TO  
FIG.  
30-3

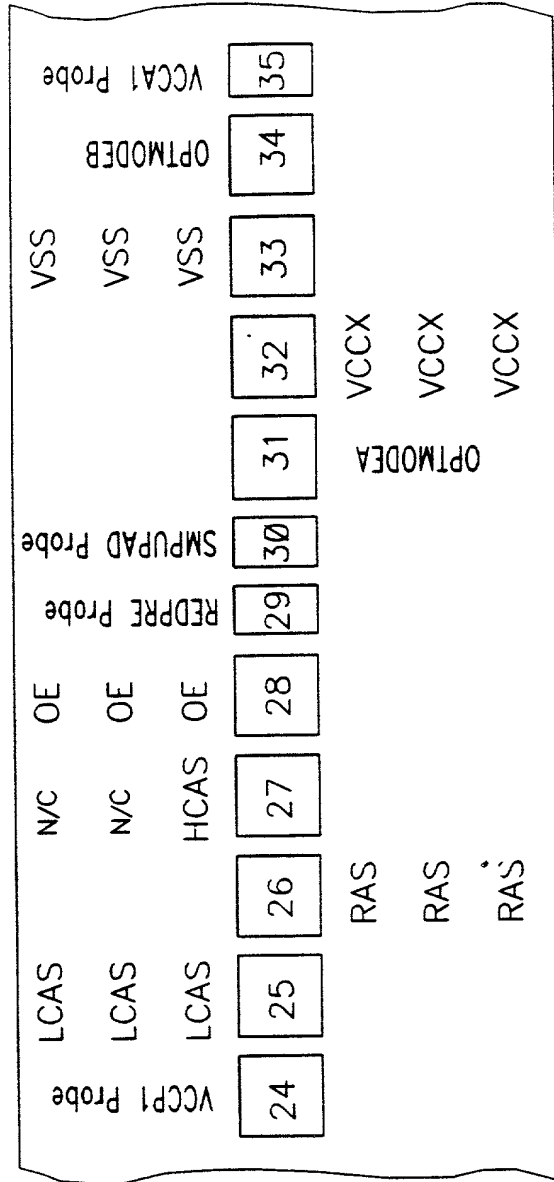
FIG 30-1

<b>X4</b>	VSSQ	N/C	VSSQ	N/C	N/C						
<b>X8</b>	VSSQ	DQ3	VSSQ	DQ2	N/C						
<b>X16</b>	VSSQ	DQ7	VSSQ	DQ6	DQ5						
	1	2	3	4	5	6	7	8	9	10	11
<b>X16</b>	VCCQ	DQ0	DQ1	VCCQ	DQ1	DQ2	VCCQ				
<b>X8</b>	VCCQ	DQ0	DQ1	VCCQ	DQ1	N/C	N/C				
<b>X4</b>	VCCQ	DQ0	DQ1	VCCQ	DQ1	N/C	N/C				

TO FIG. 31A2

FIG. 31A1






TO FIG. 31B2

FIG. 31B1



TO FIG. 31B1  


A13	A12	A11	A10	A9
A13	A12	A11	A10	A9
A13	A12	A11	A10	A9
36	37	38	39	40
41	42	43	44	45
46				
A0	A1	A2	A3	A4
A0	A1	A2	A3	A4
A0	A1	A2	A3	A4
				A5
				A5
				A5

FIG. 31B2

FIG. 31C1

TO FIG. 31C2

T0 FIG. 31C1

N/C	N/C	N/C	VSSQ	N/C	N/C	VSSQ	VBB
N/C	DQ6	N/C	VSSQ	N/C	N/C	VSSQ	VBB
VSSQ	DQ14	DQ13	VSSQ	DQ12	VSSQ	VSSQ	VBB
60	61	62	63	64	65	66	67
DQ9	DQ10	VCCQ	DQ11	VCCQ	VCCQ	VCCQ	VBB
DQ5	N/C	VCCQ	N/C	VCCQ	VCCQ	VCCQ	VBB
DQ3	N/C	VCCQ	N/C	VCCQ	VCCQ	VCCQ	VBB

FIG. 31C2

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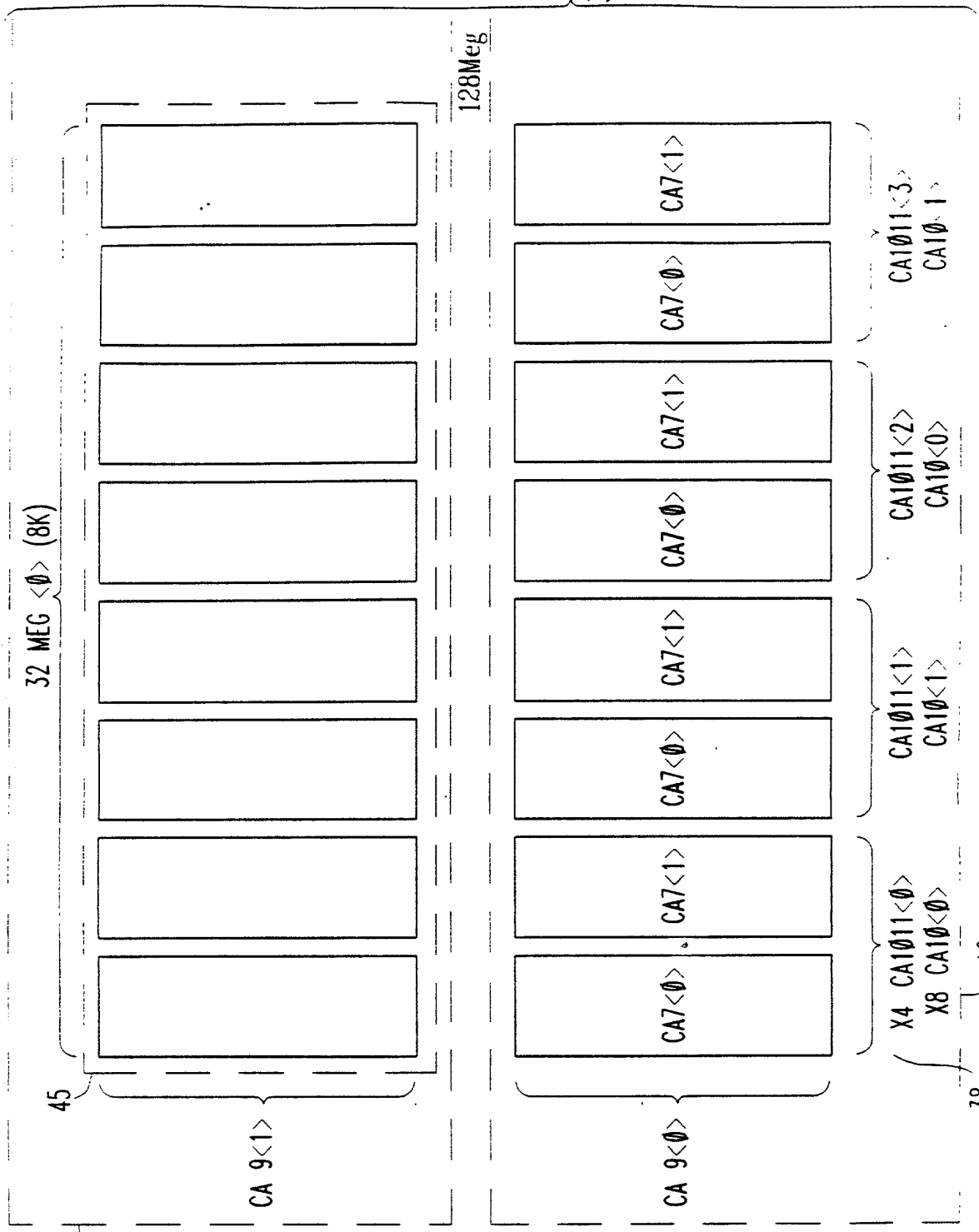


FIG. 32A1

TO  
FIG.  
32A3

PART TYPE	32MEG
ANY 16K	RA 13
X4 8K OR 4K	CA 12
X8 8K OR 4K	CA 11
X16 8K OR 4K	CA 10

FIG. 32A2

$\left\{ \begin{array}{l} \text{CA } 6 < \emptyset:1 > \text{ MSB} \\ \text{CA } 45 < \emptyset:3 > \\ \text{CA } 23 < \emptyset:3 > \\ \text{CA } \emptyset 1 < \emptyset:3 > \\ \text{CA } 8 < \emptyset:1 > \text{ LSB} \end{array} \right.$

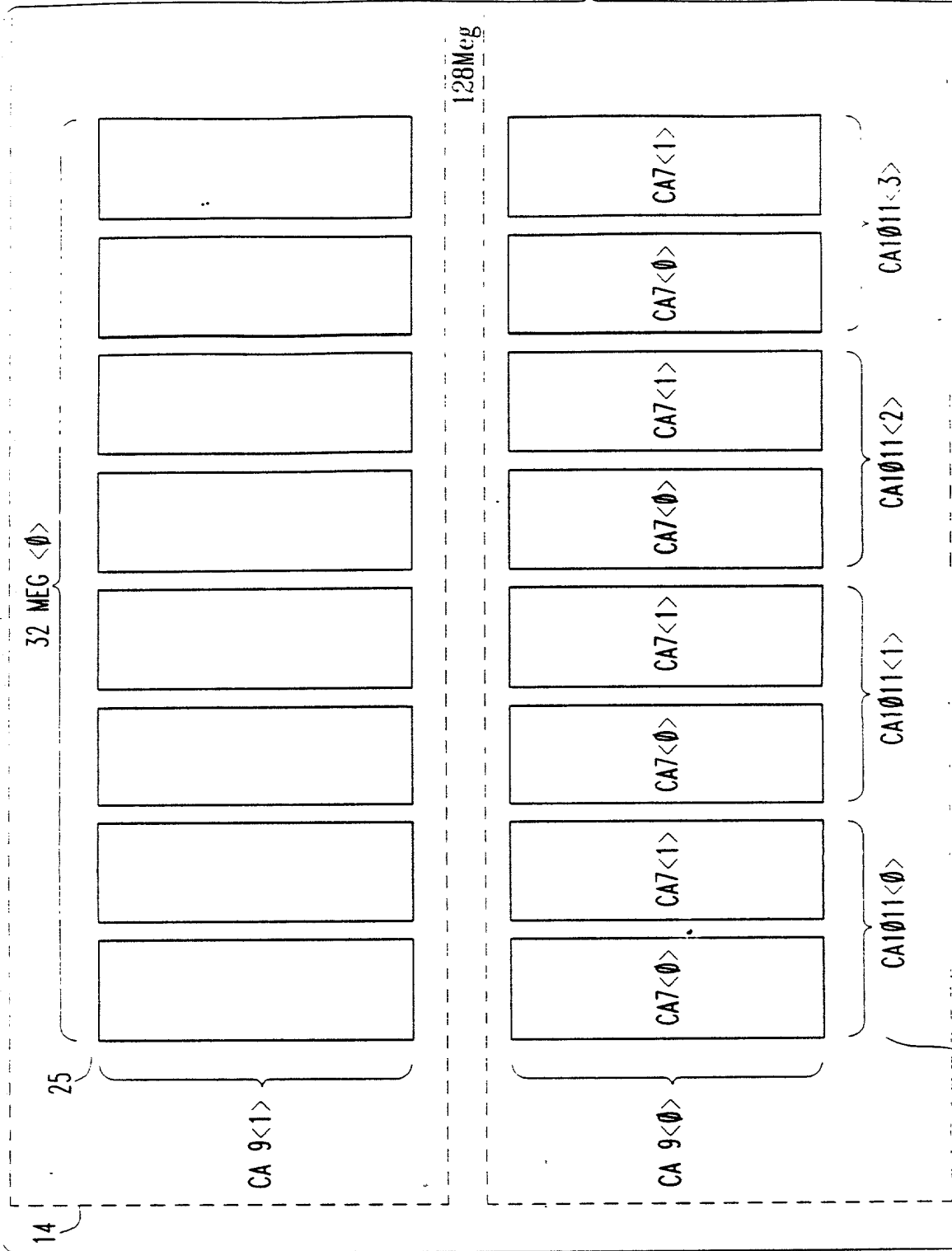
32 MEG <1> (8K)

47

FROM  
FIG.  
32A1

LSB → MSB

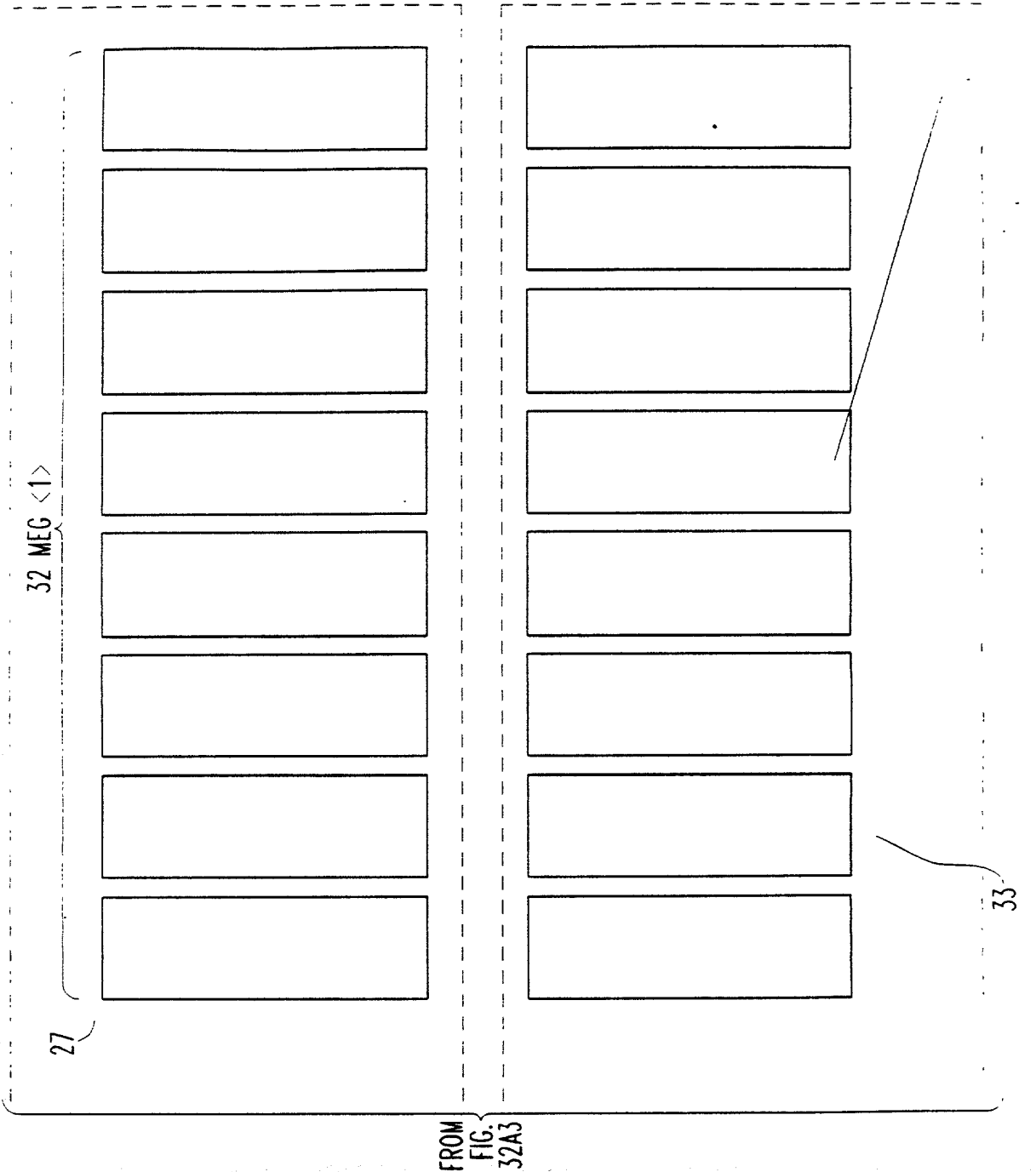
40



FROM  
FIG.  
32A2

FIG. 32A3

FIG. 32A4



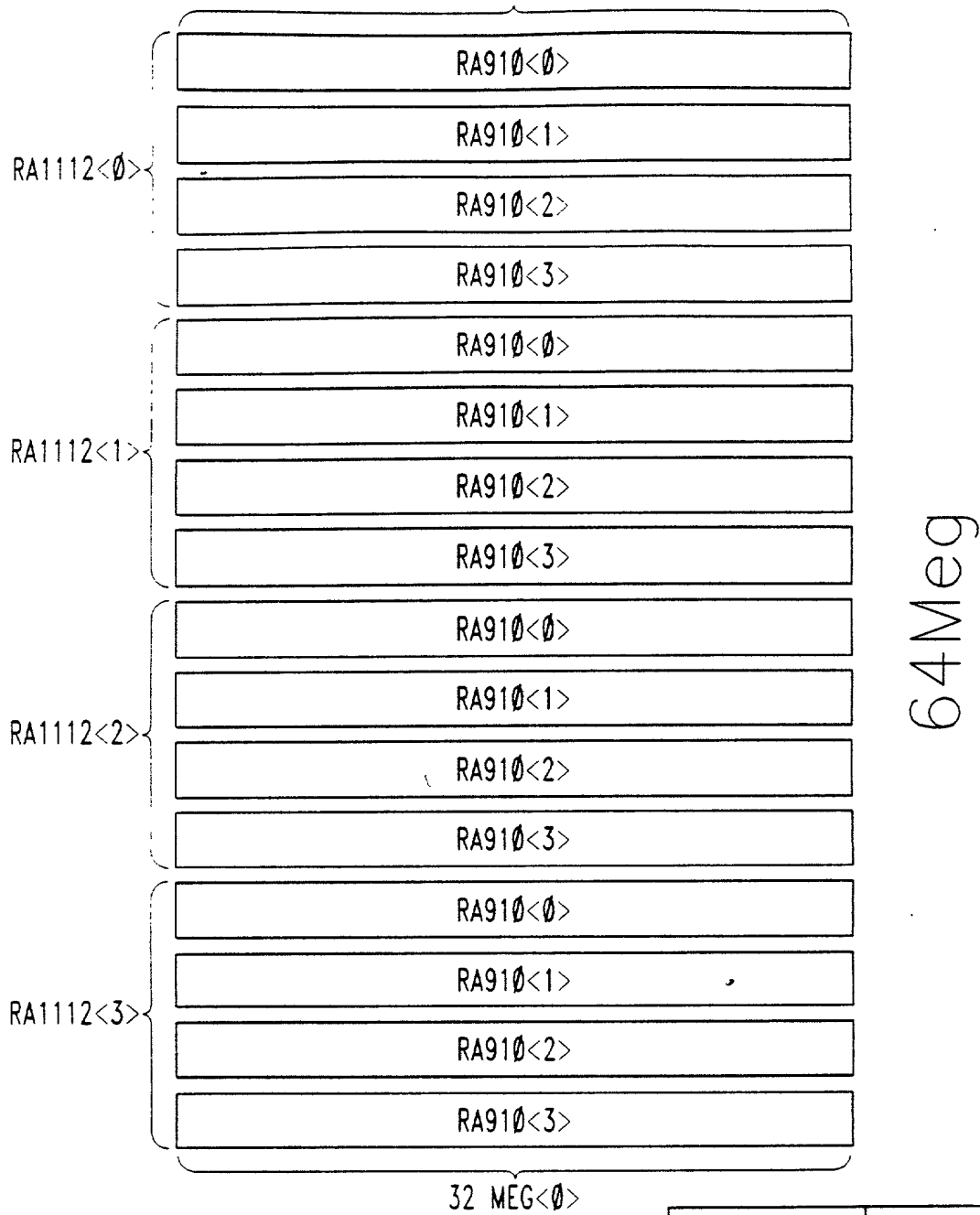


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10



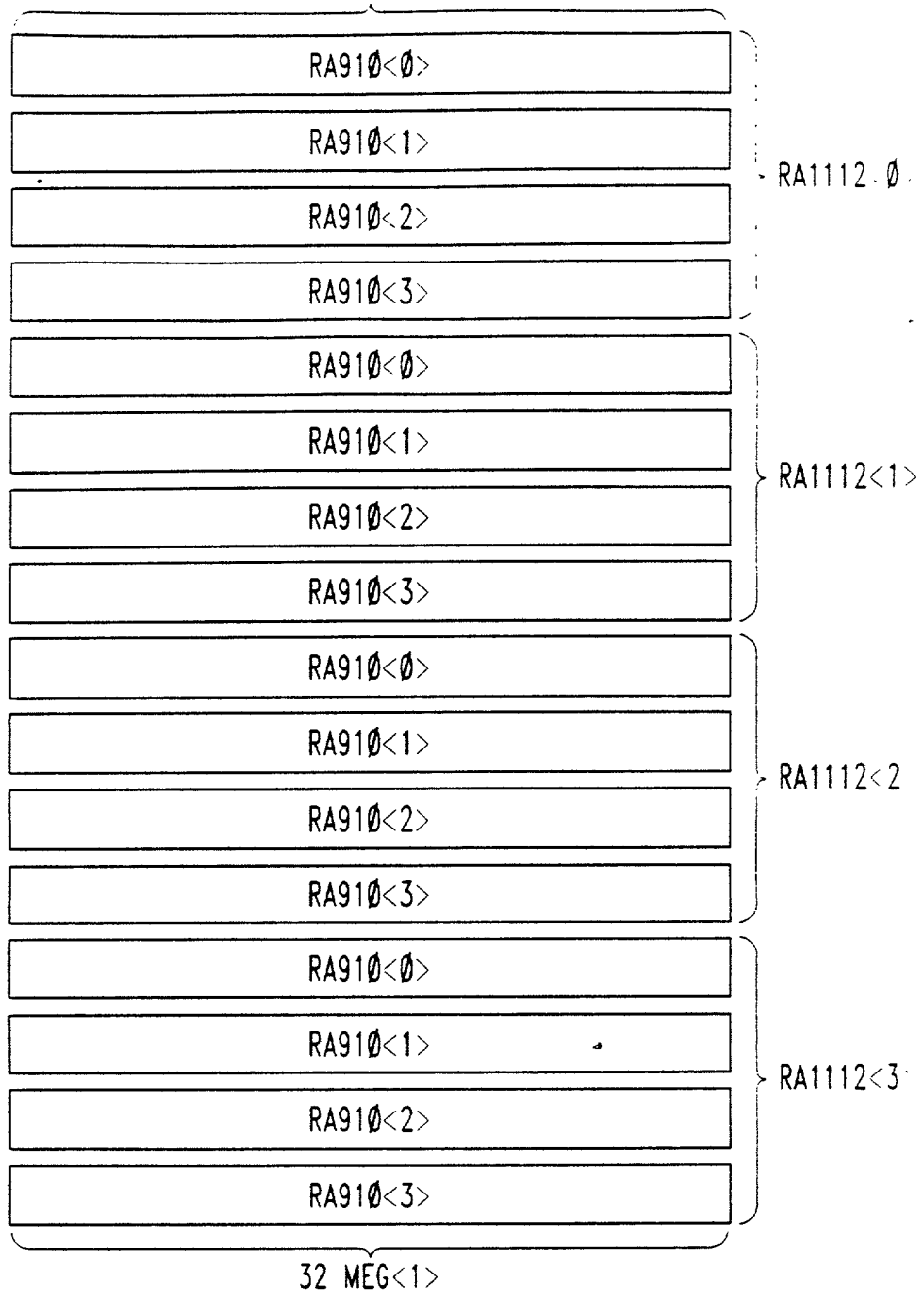
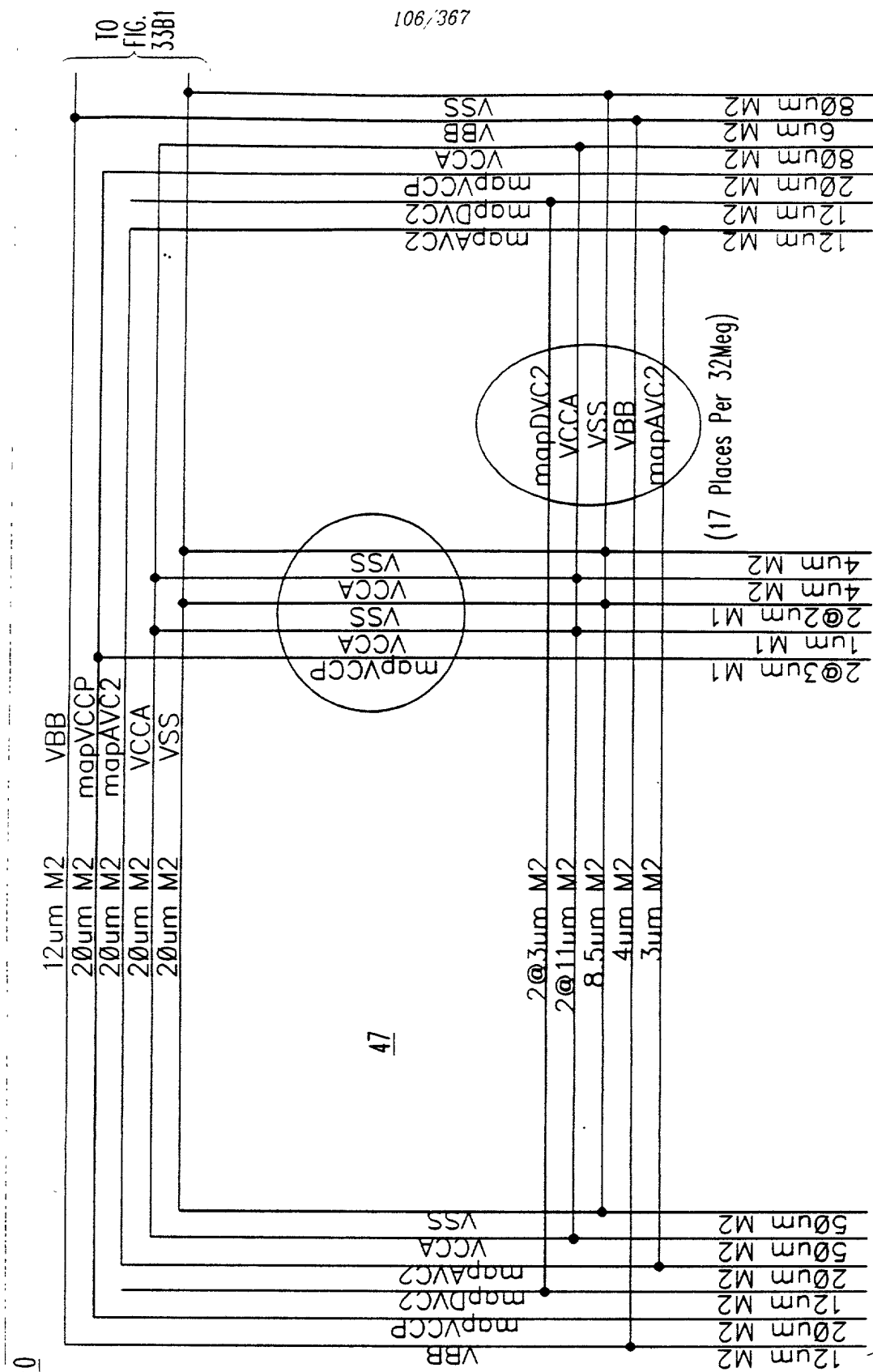


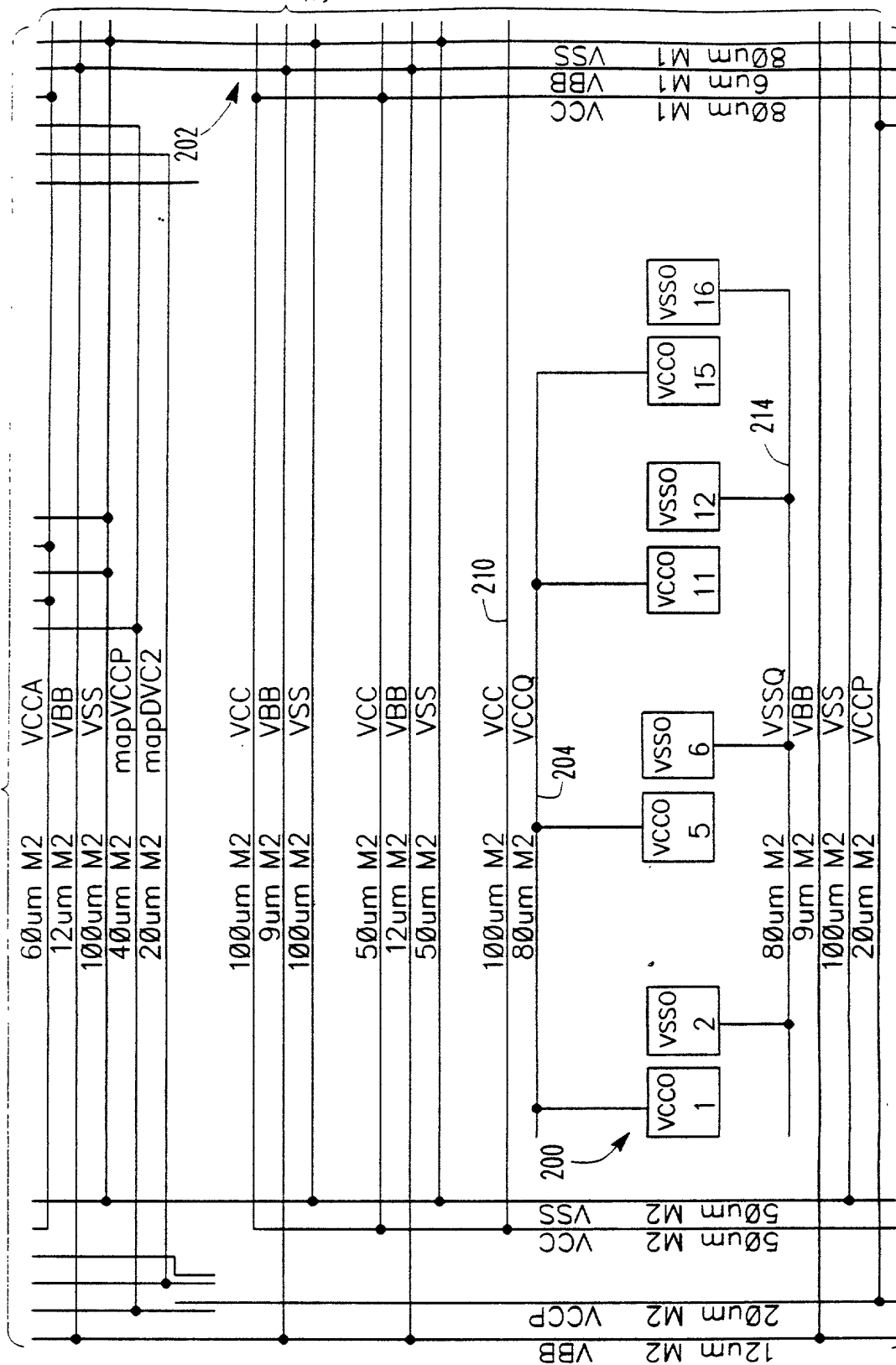
FIG. 32B2



TO FIG. 33A2

FIG 33A

FROM FIG. 33A1

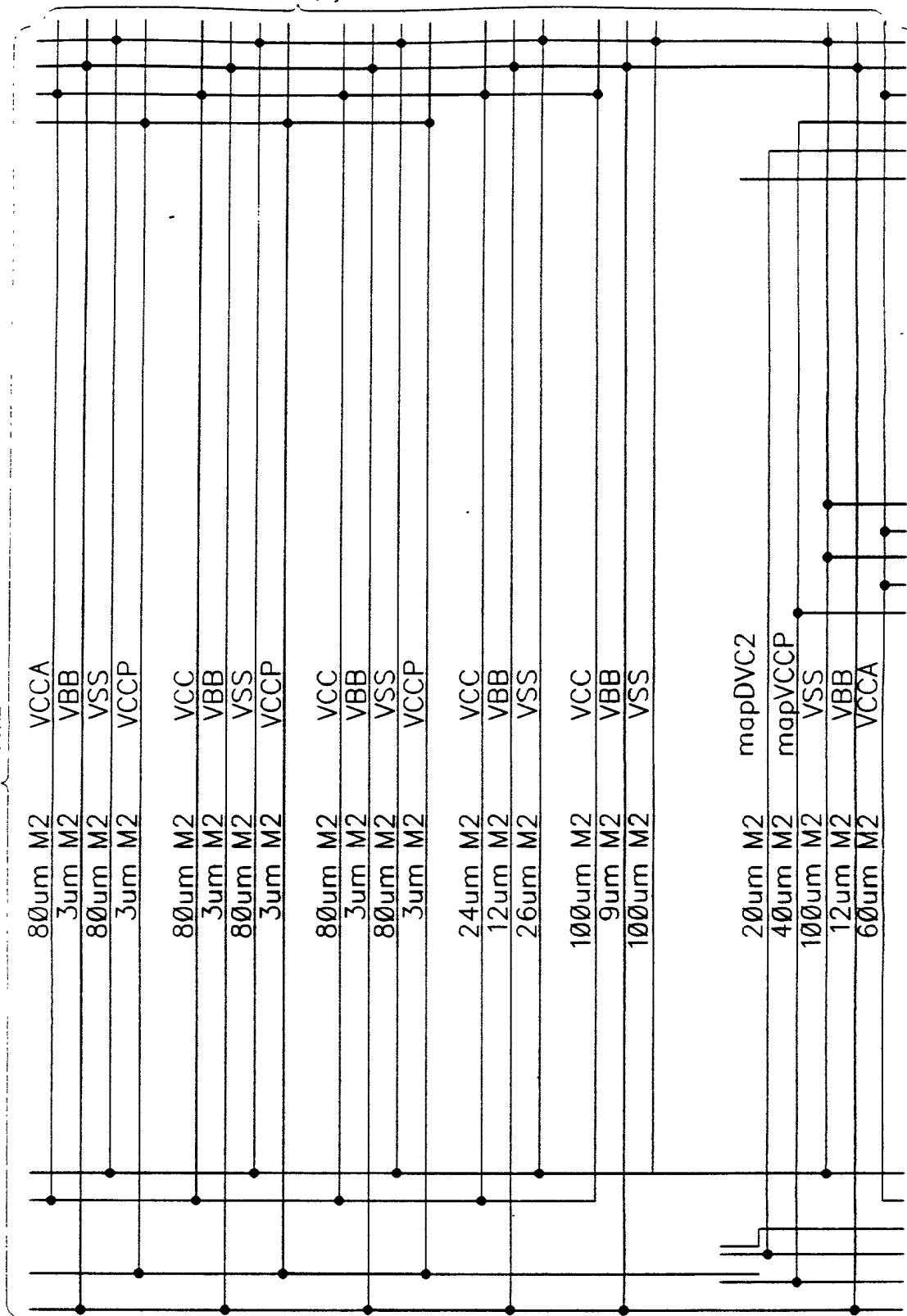


TO FIG. 33A3

U/C 3342

[illegible]

FROM FIG. 33A2



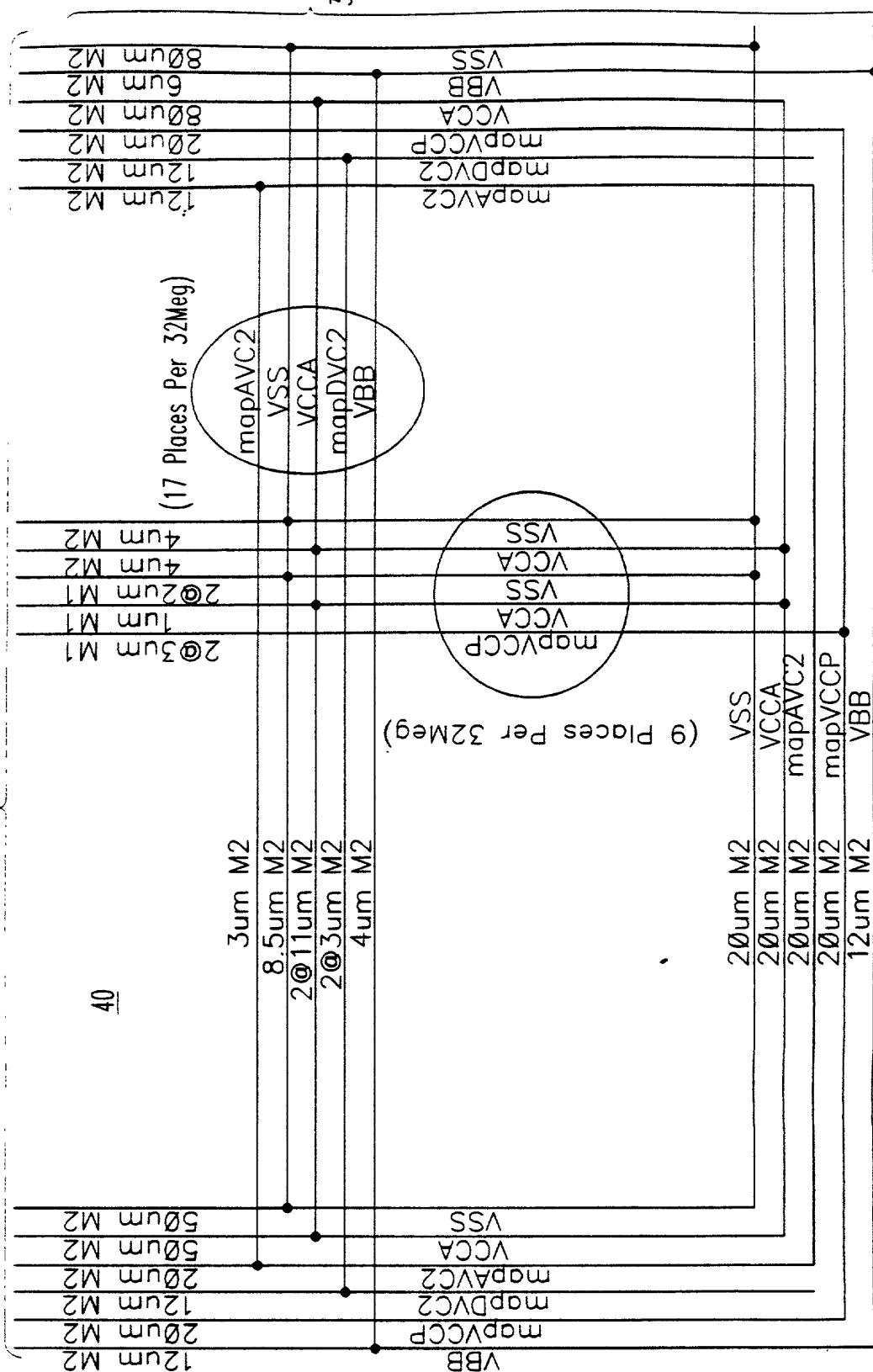
TO FIG. 33A4

U/C 3343

TO  
FIG.  
3385

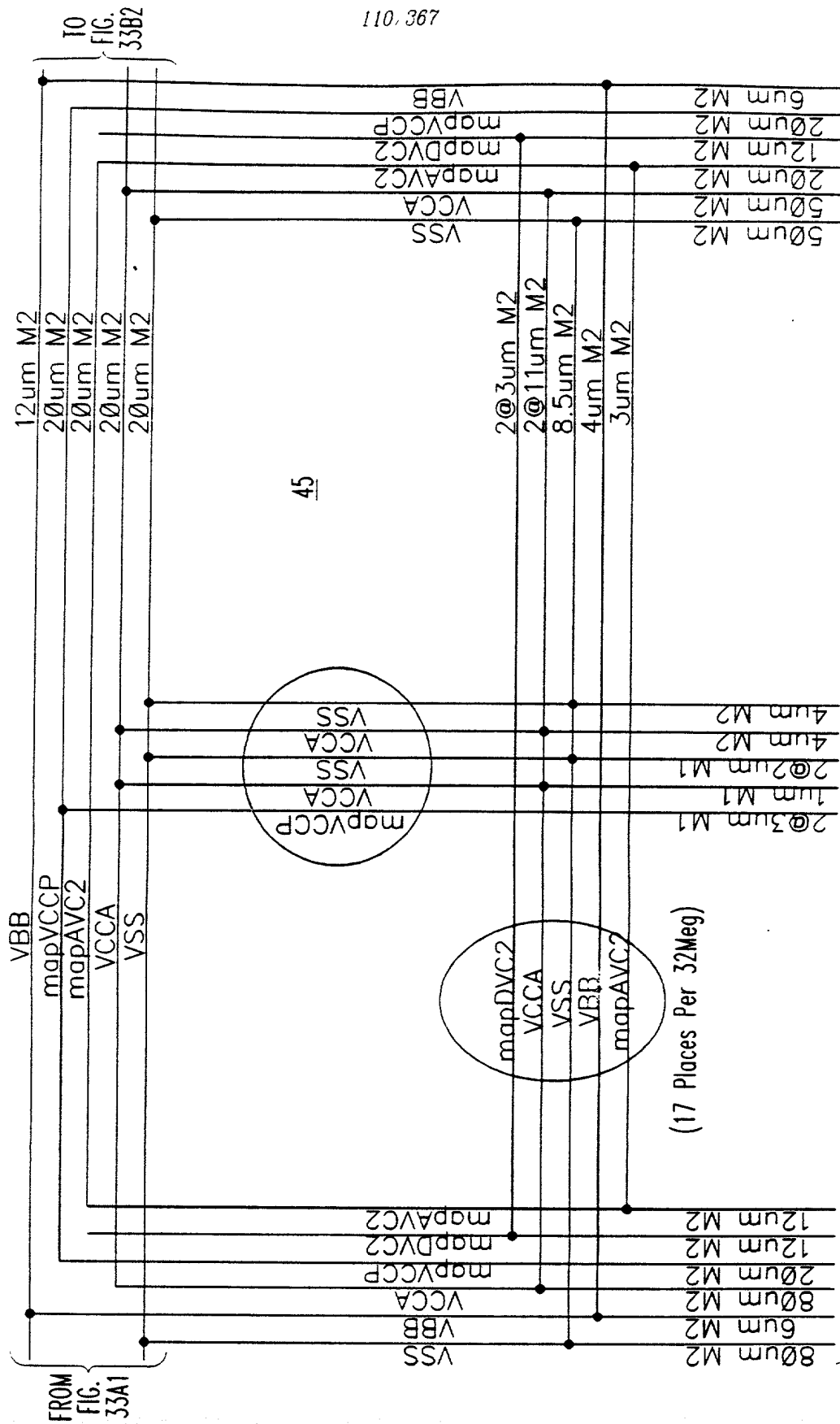
108,367

FROM FIG. 33A3



1163311

FIG. 33B1



110.367

10 FIG. 33B3

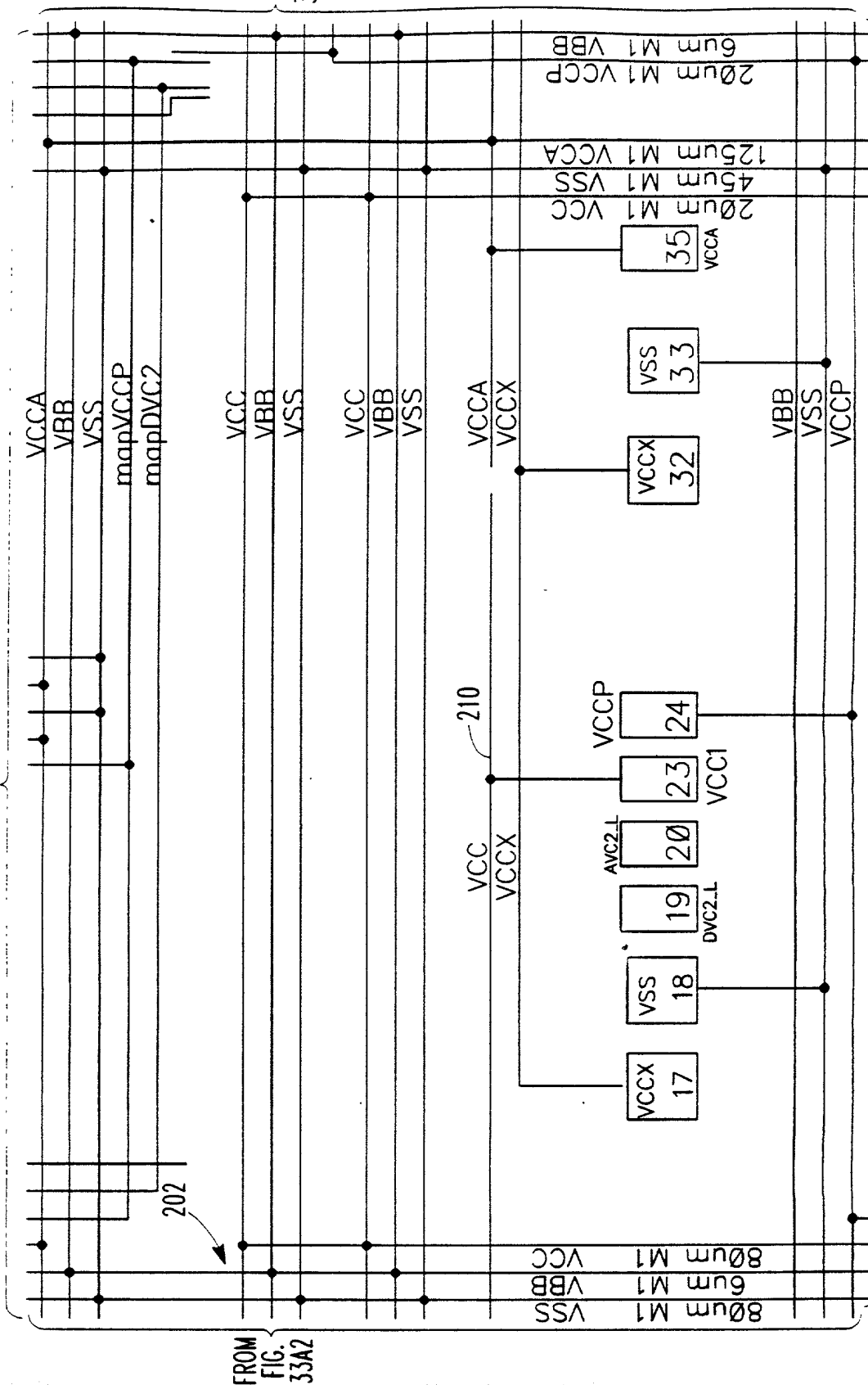
FIG. 33B1



FIG. 33B2

FIG. 33B1

FROM FIG. 33B1



FROM FIG. 33A2

FIG. 33B4

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TO FIG. 33B3

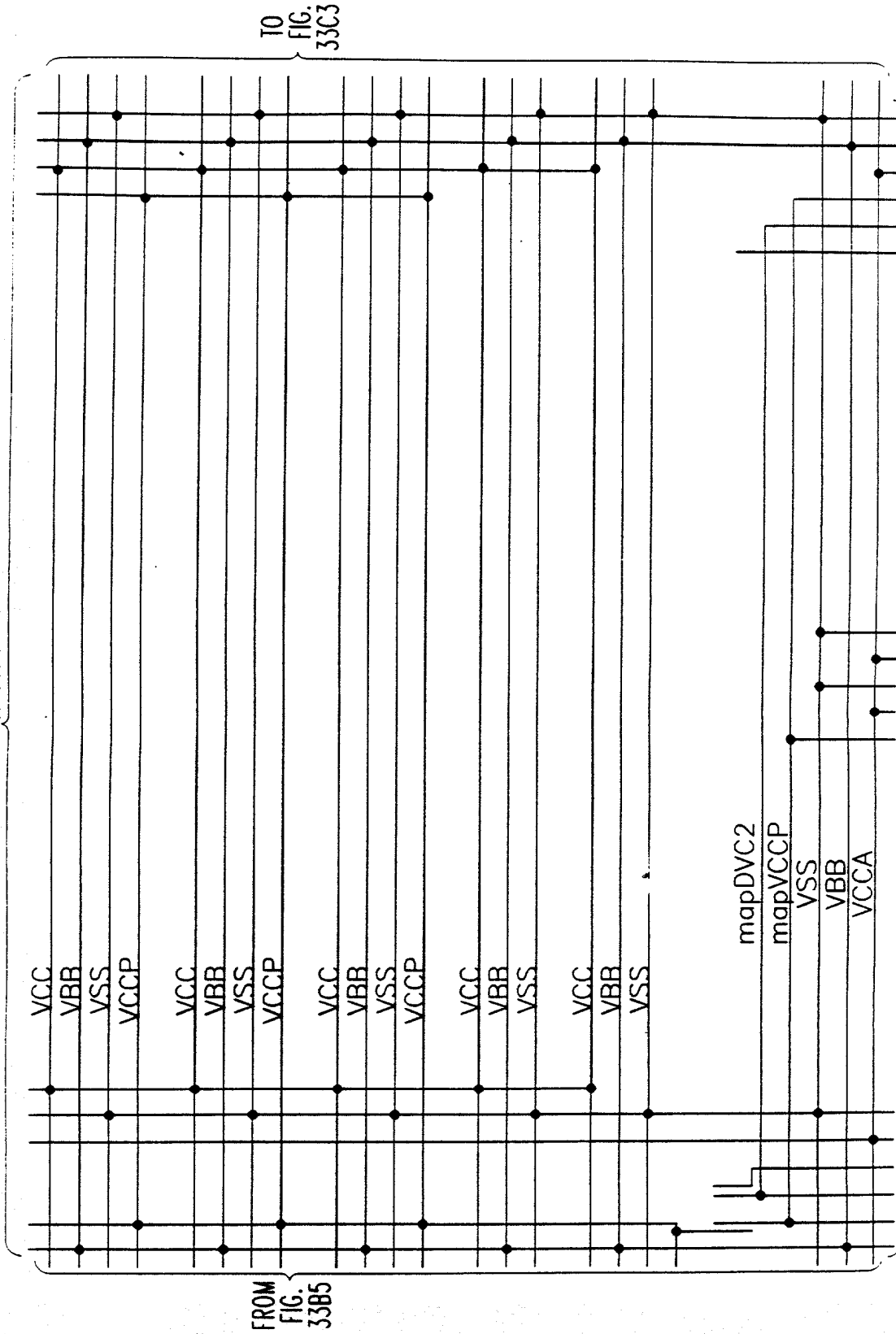
FIG. 33B3







FROM FIG. 33B4



TO FIG. 33B8

FIG. 33B6

FROM FIG. 33B5

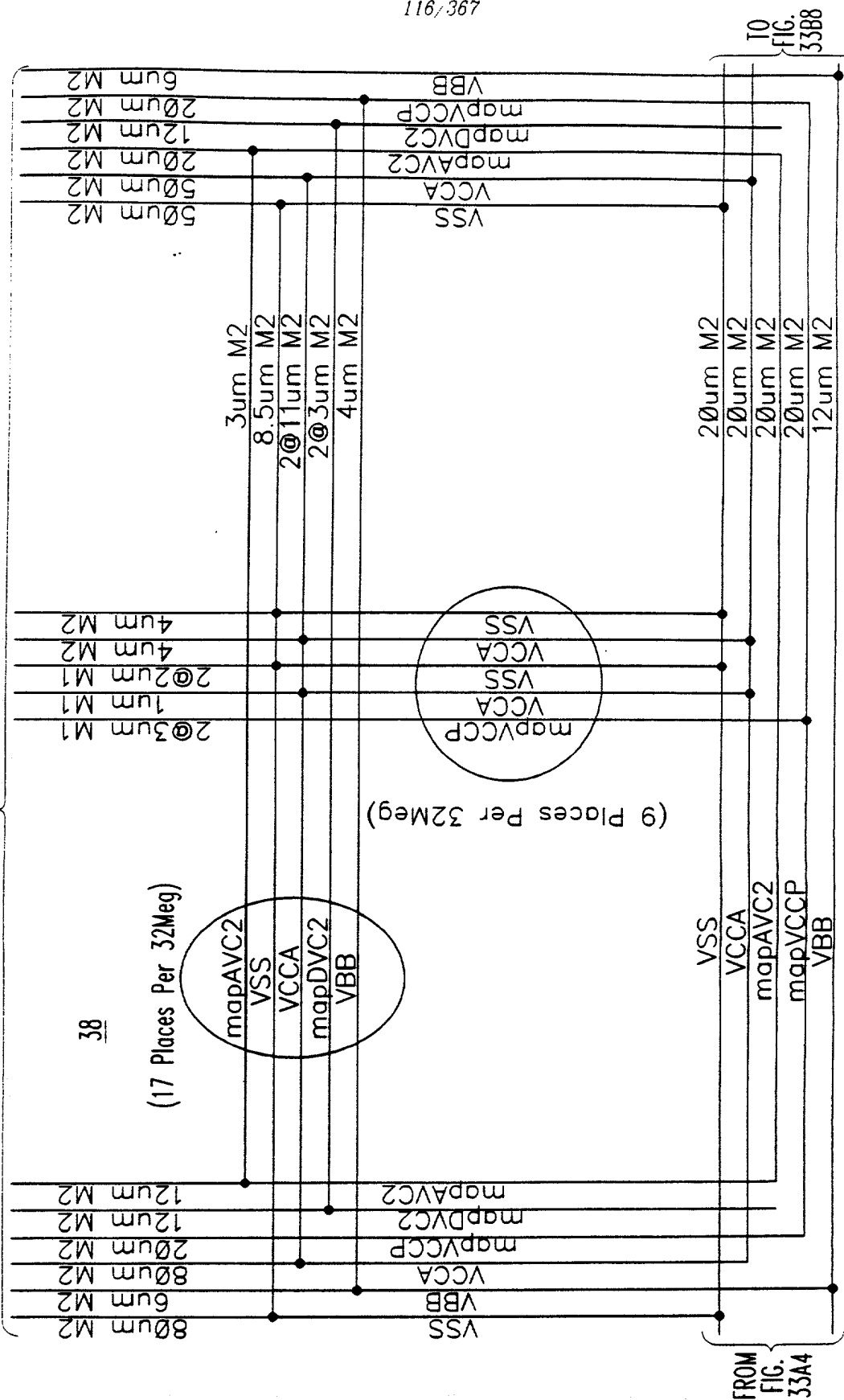
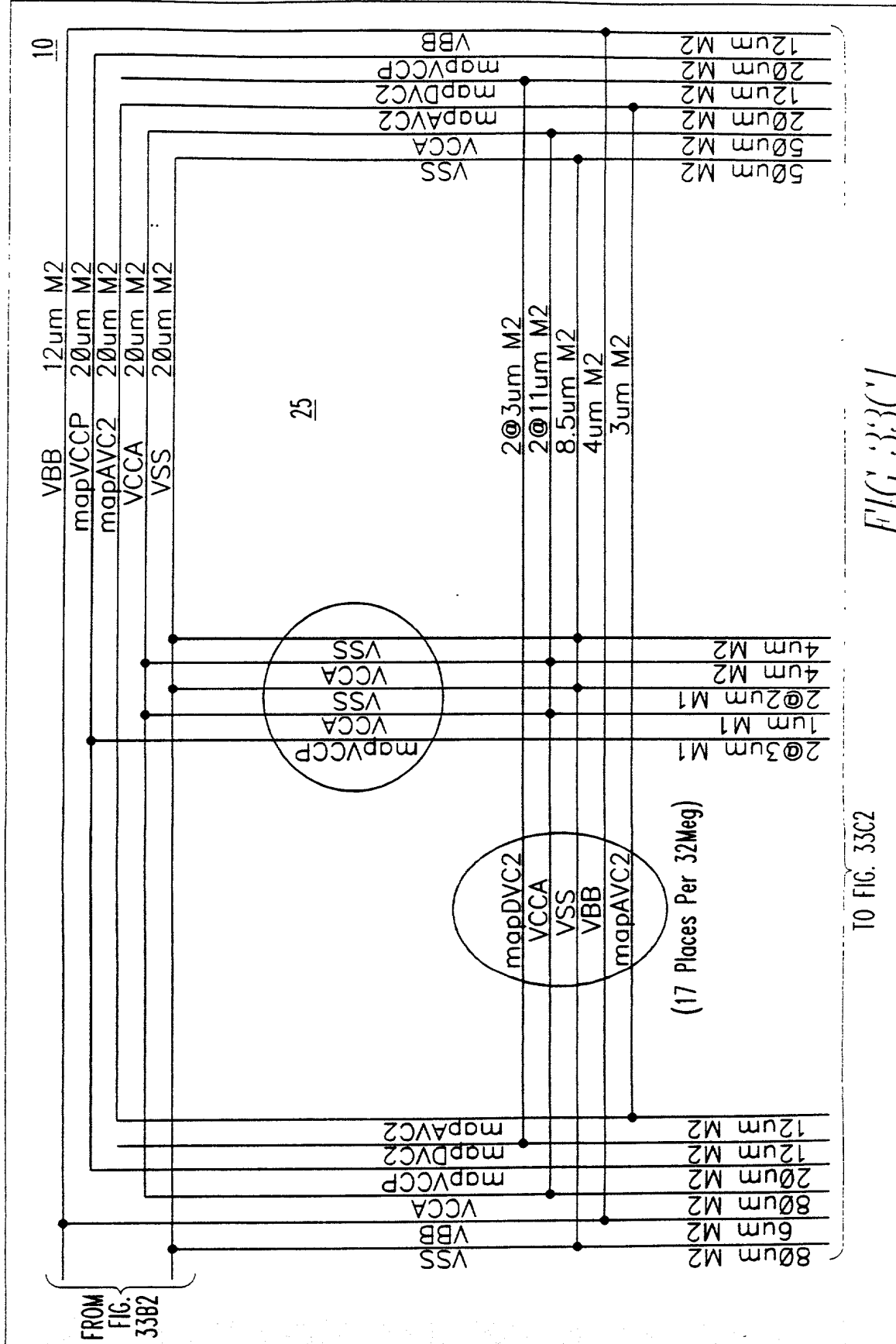


FIG. 33B7





TO FIG. 33C2

FIG. 33C1

FROM  
FIG.  
3383

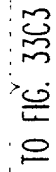
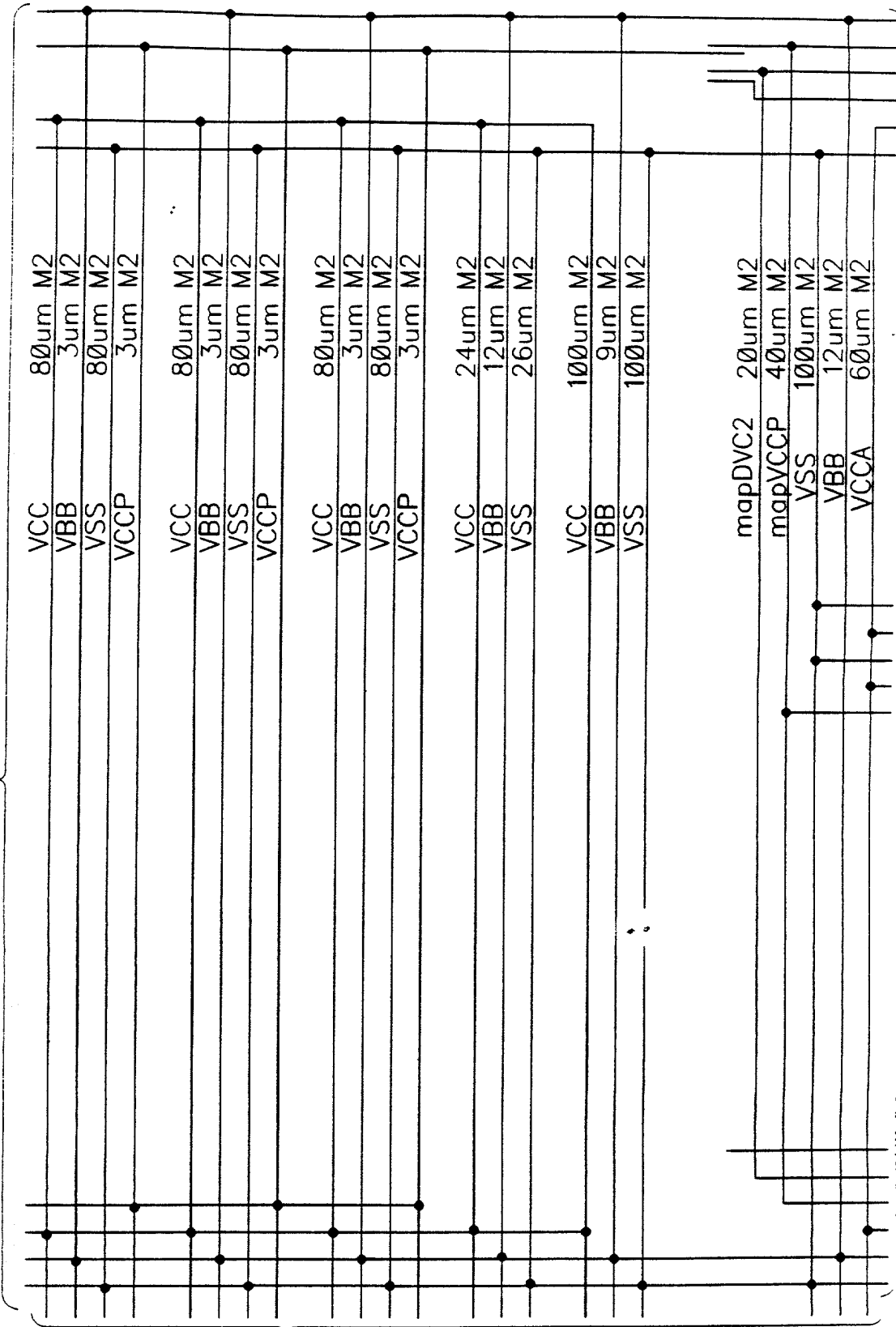


FIG. 33C2

FROM  
FIG.  
33B6



TO FIG. 33C4

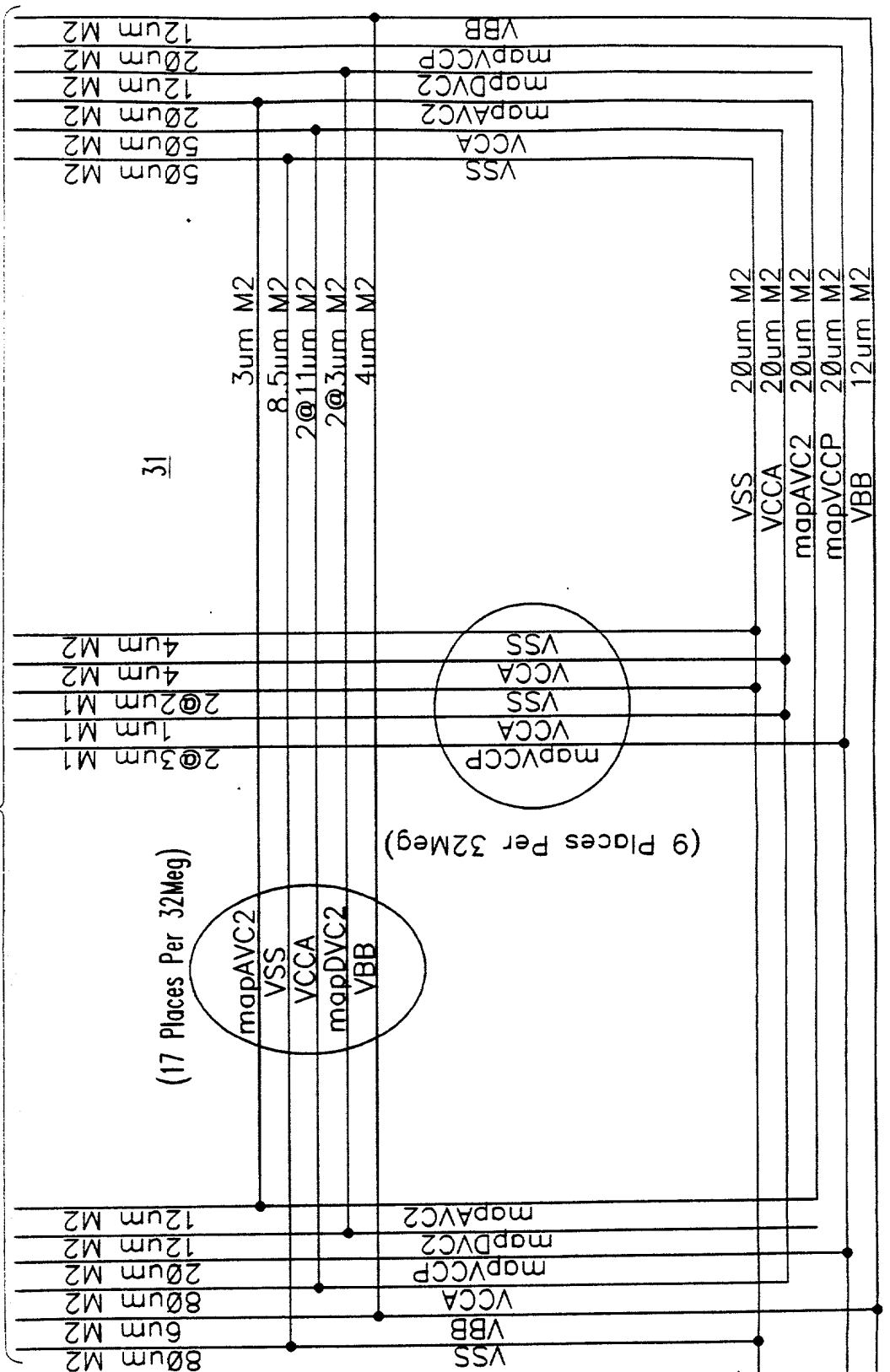
1763



31

(17 Places Per 32Meg)

(9 Places Per 32Meg)

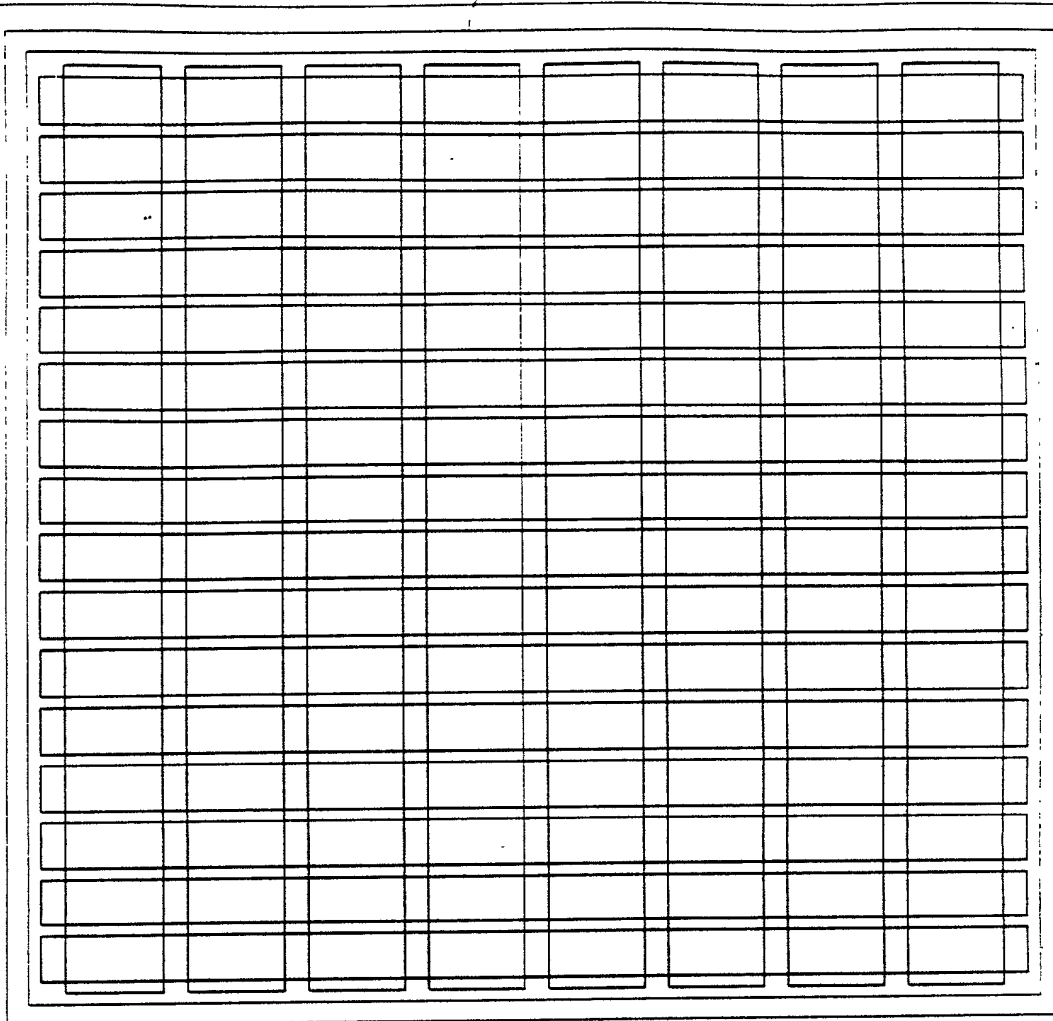


FROM  
FIG.  
33B8

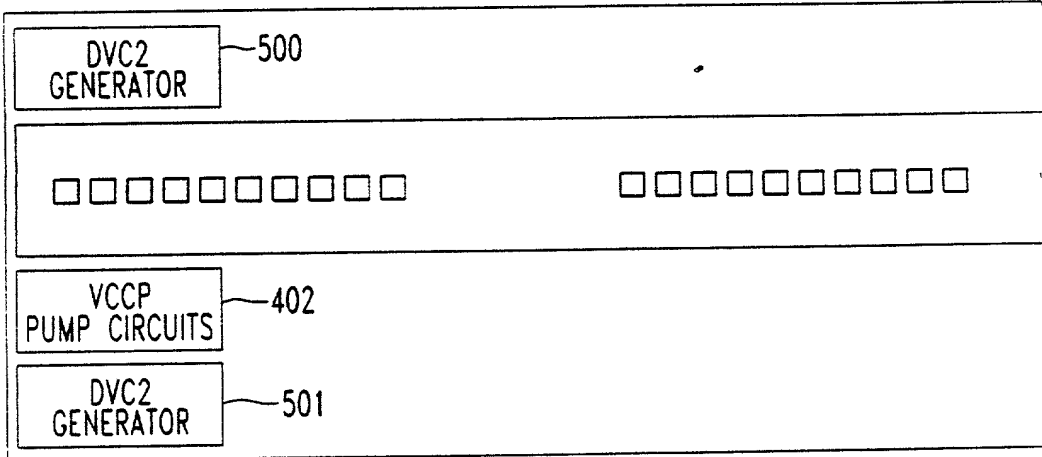
11/6/33

10

45



200

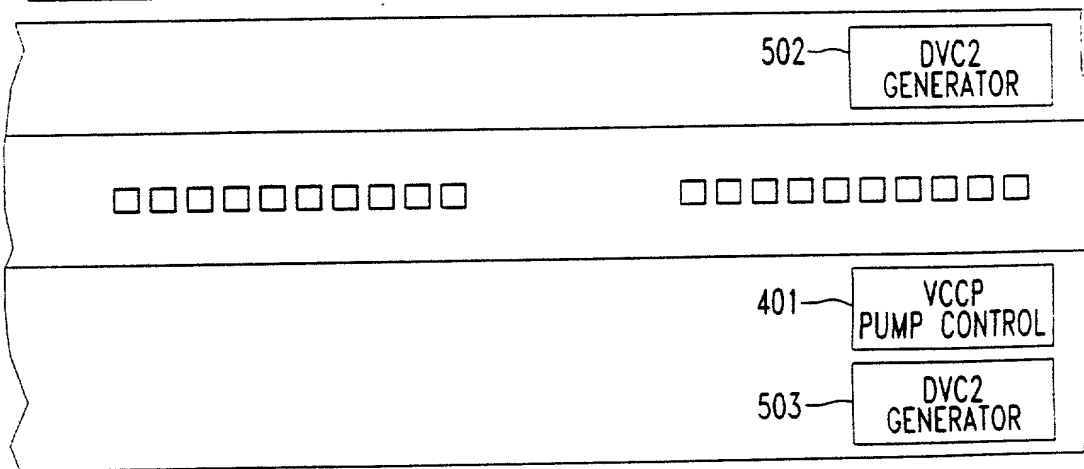
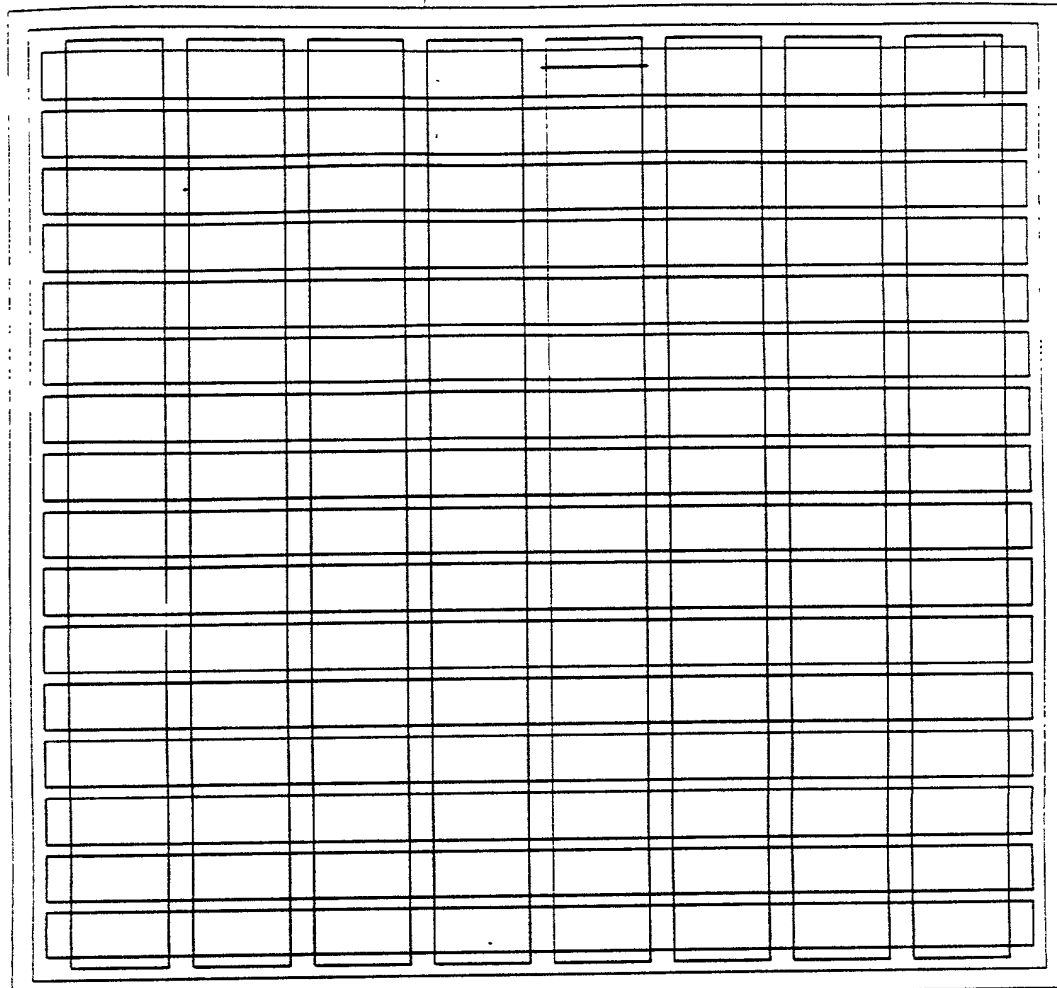
TO  
FIG.  
33D3

TO FIG. 33D2

FIG. 33D1

TO FIG. 33D1

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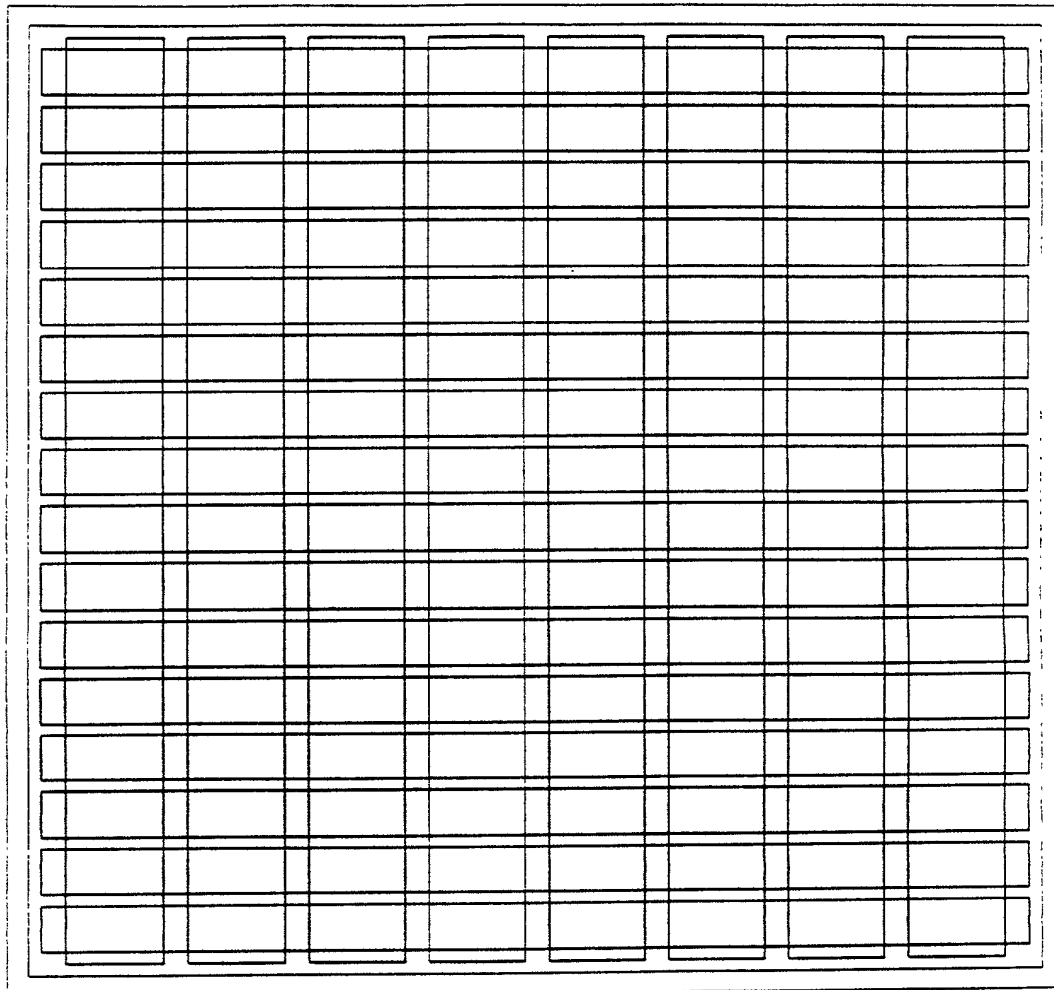


TO  
FIG.  
▼ 33D4

FIG. 33D2

TO  
FIG.  
33D1

(SEE FIG. 33E1)

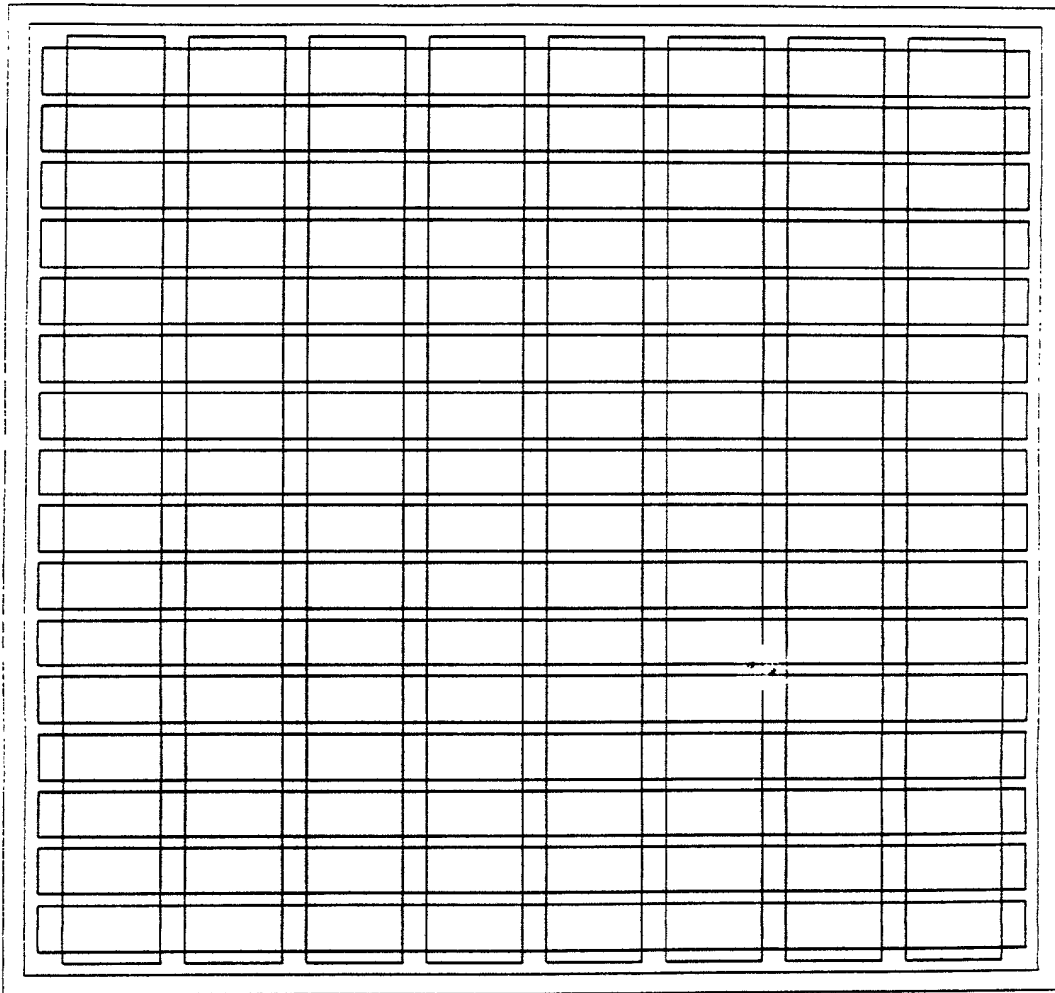


TO FIG. 33D4

FIG. 33D3

125, 367

TO  
FIG.  
33D2



40

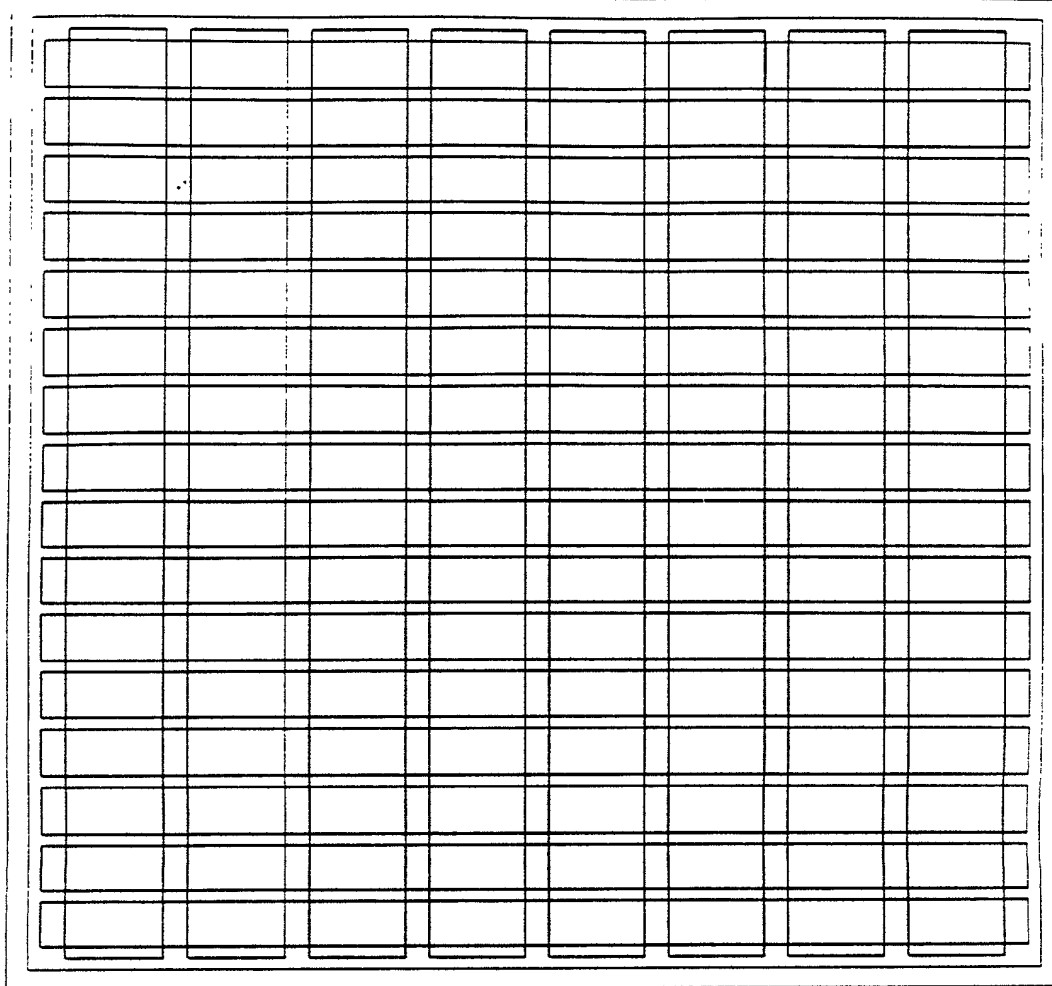
TO FIG. 33D3

FIG. 33D4

(SEE FIG. 33D2)

25

TO FIG. 33E2



DVC2  
GENERATOR 504

□ □ □ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □ □ □

VCCP  
REGULATOR 220

DVC2  
GENERATOR 505

TO  
FIG.  
33E3

FIG. 33E1

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TO FIG. 33E1

27

10

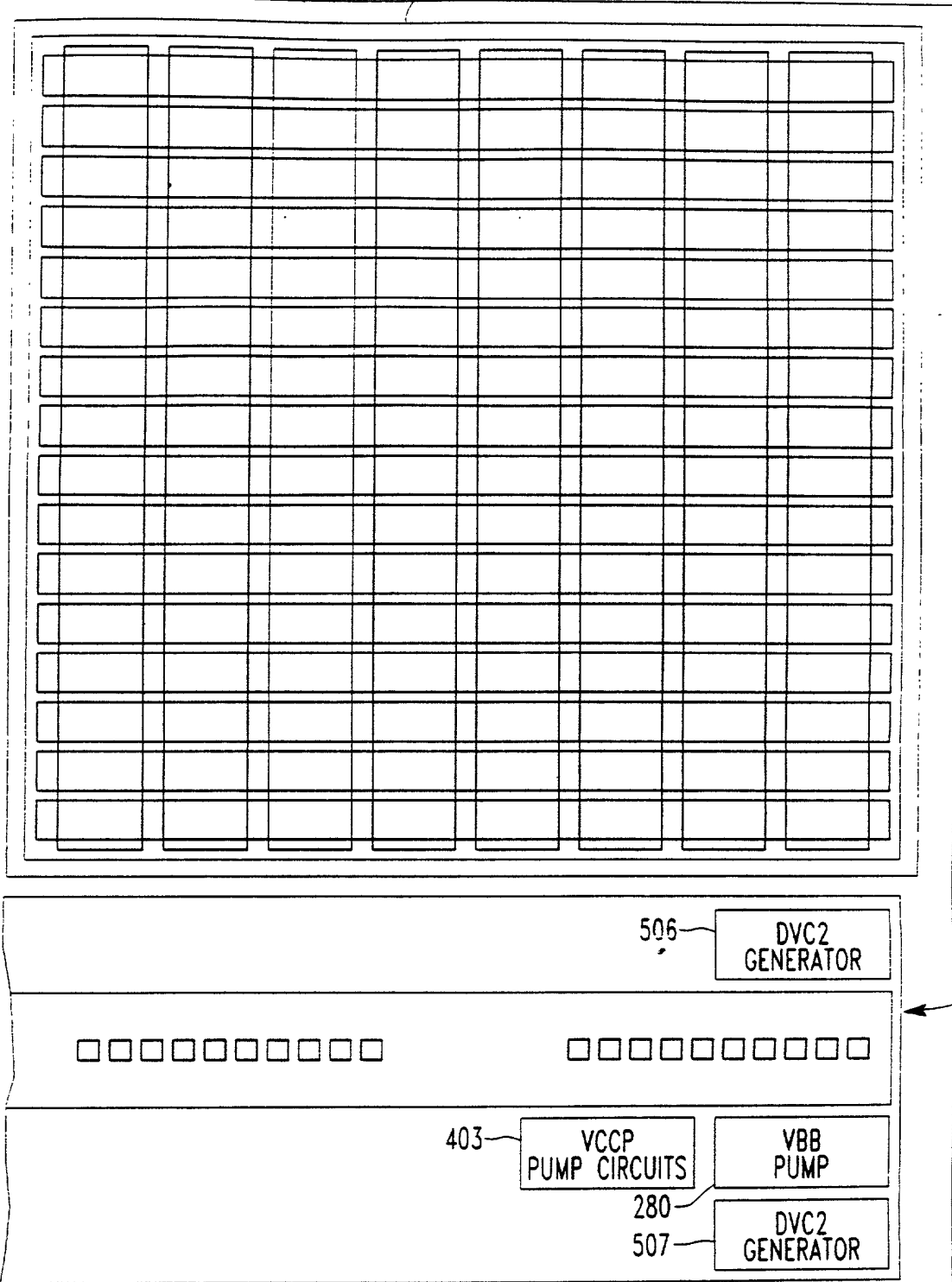
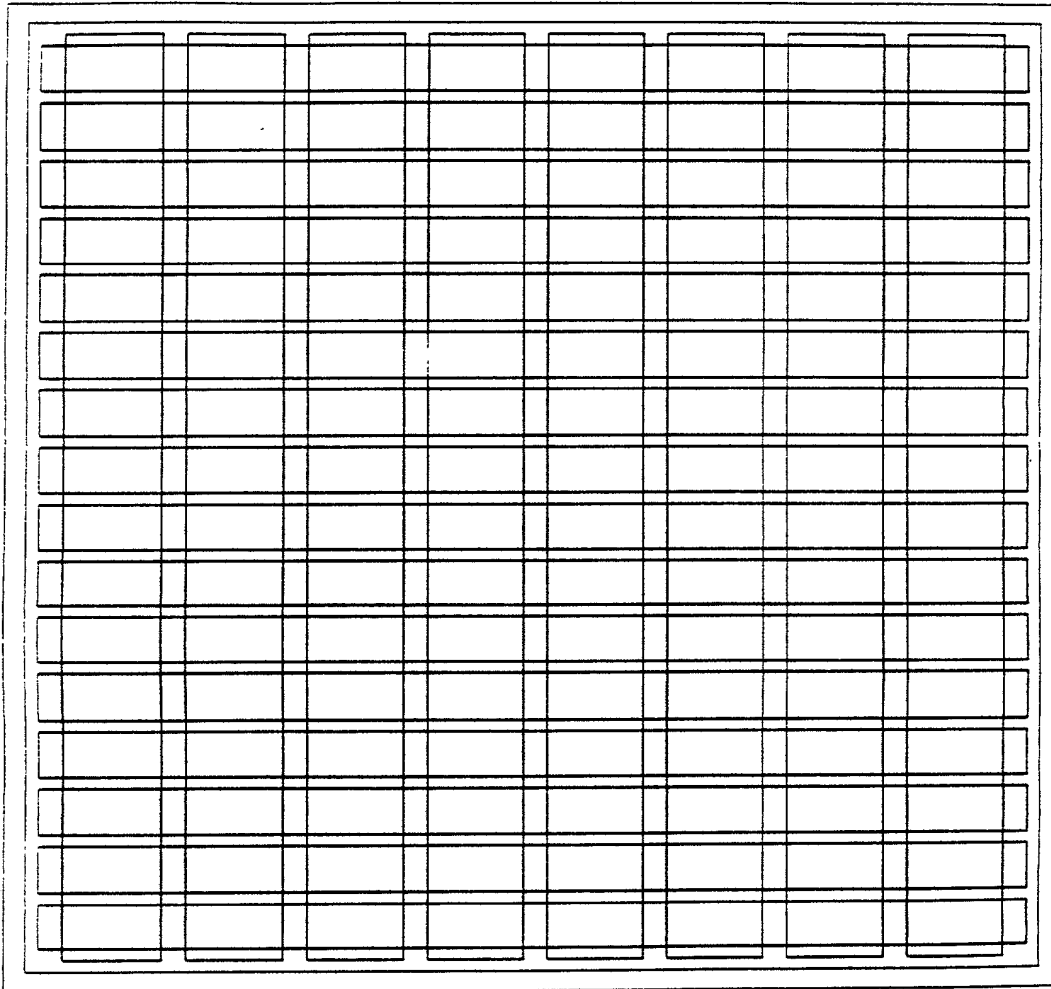


FIG. 33E2

TO  
FIG.  
33E4

TO  
FIG.  
33E1



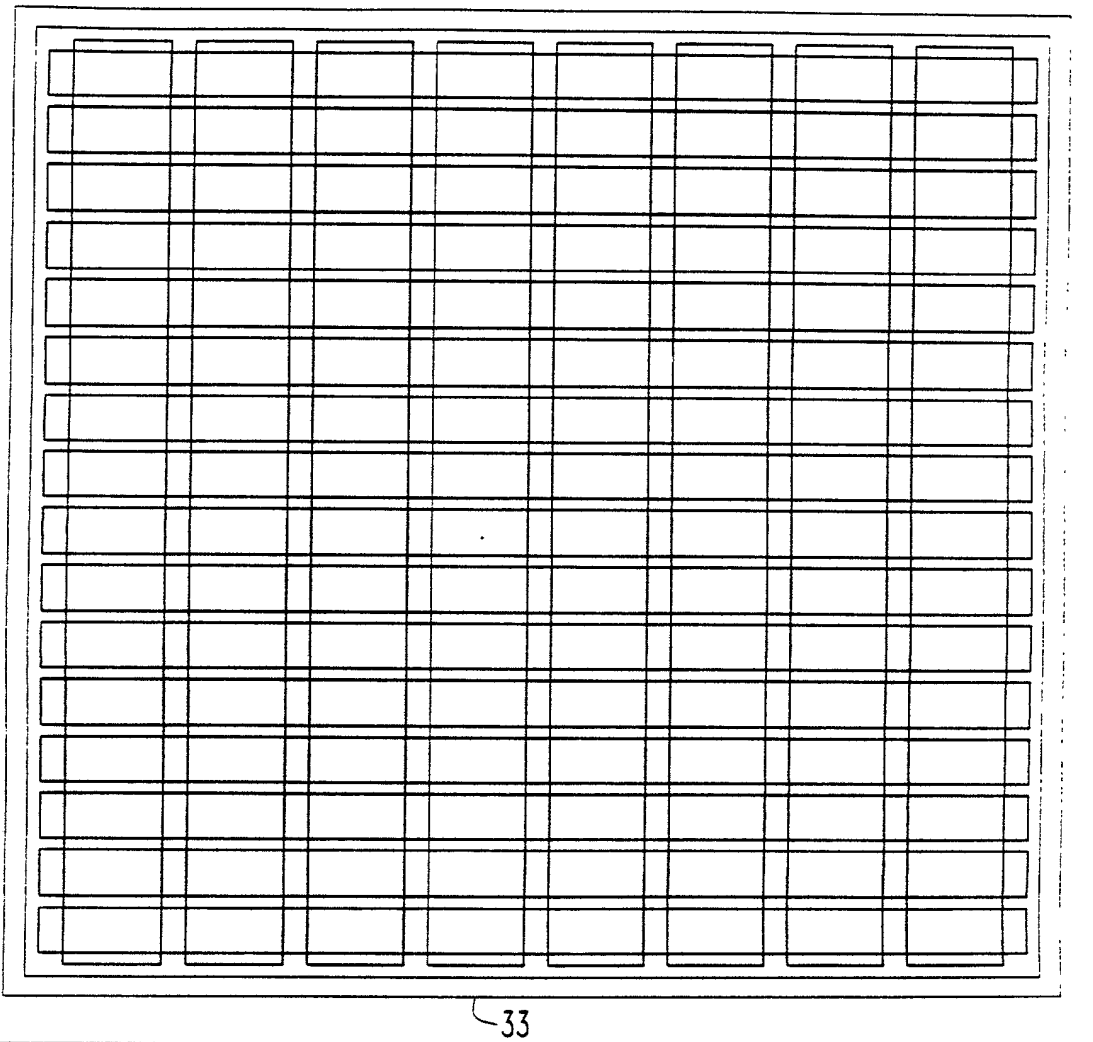
31

TO FIG. 33E4

FIG. 33E3

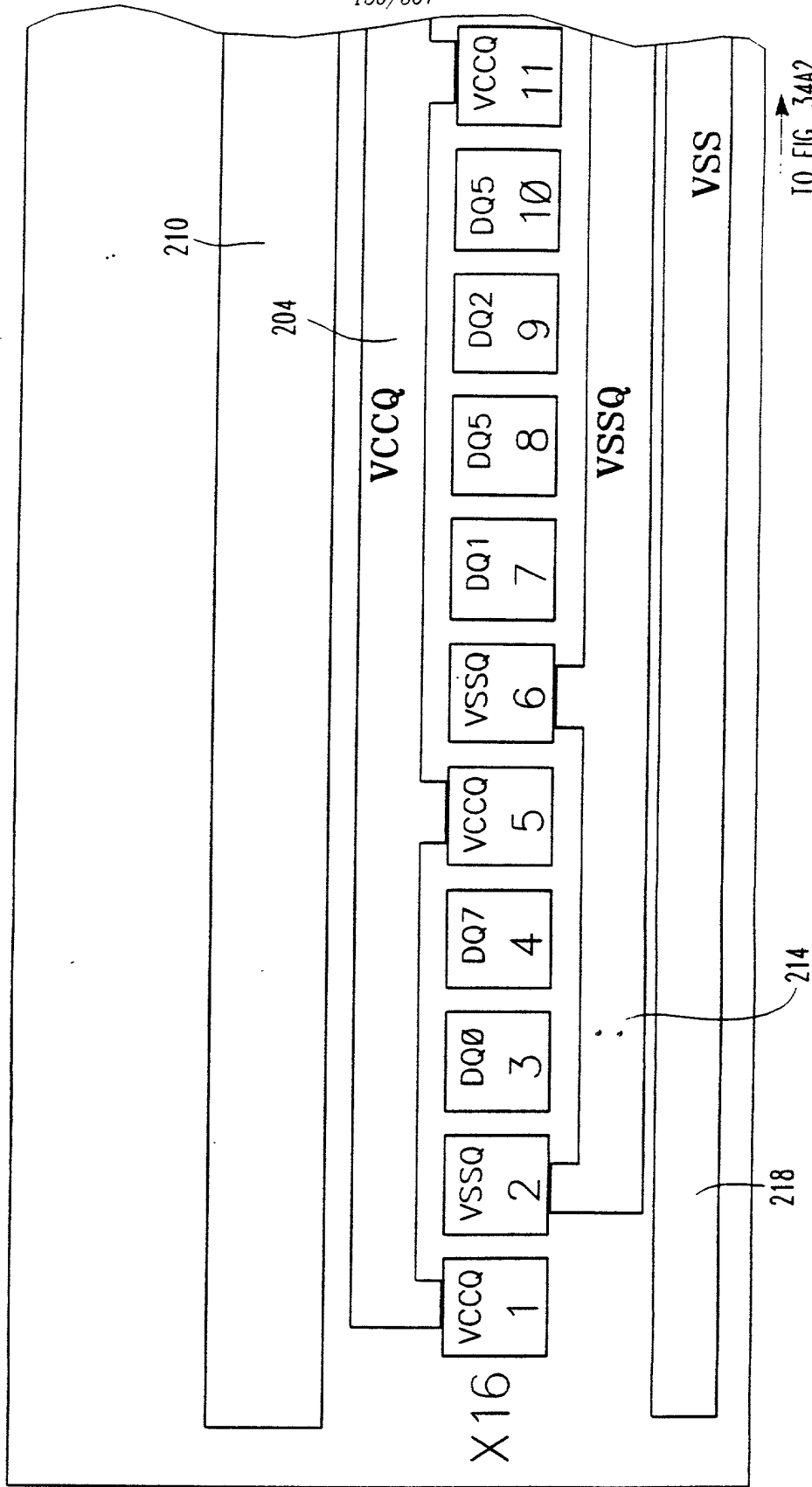


TO  
FIG.  
33E2



TO FIG. 33E3

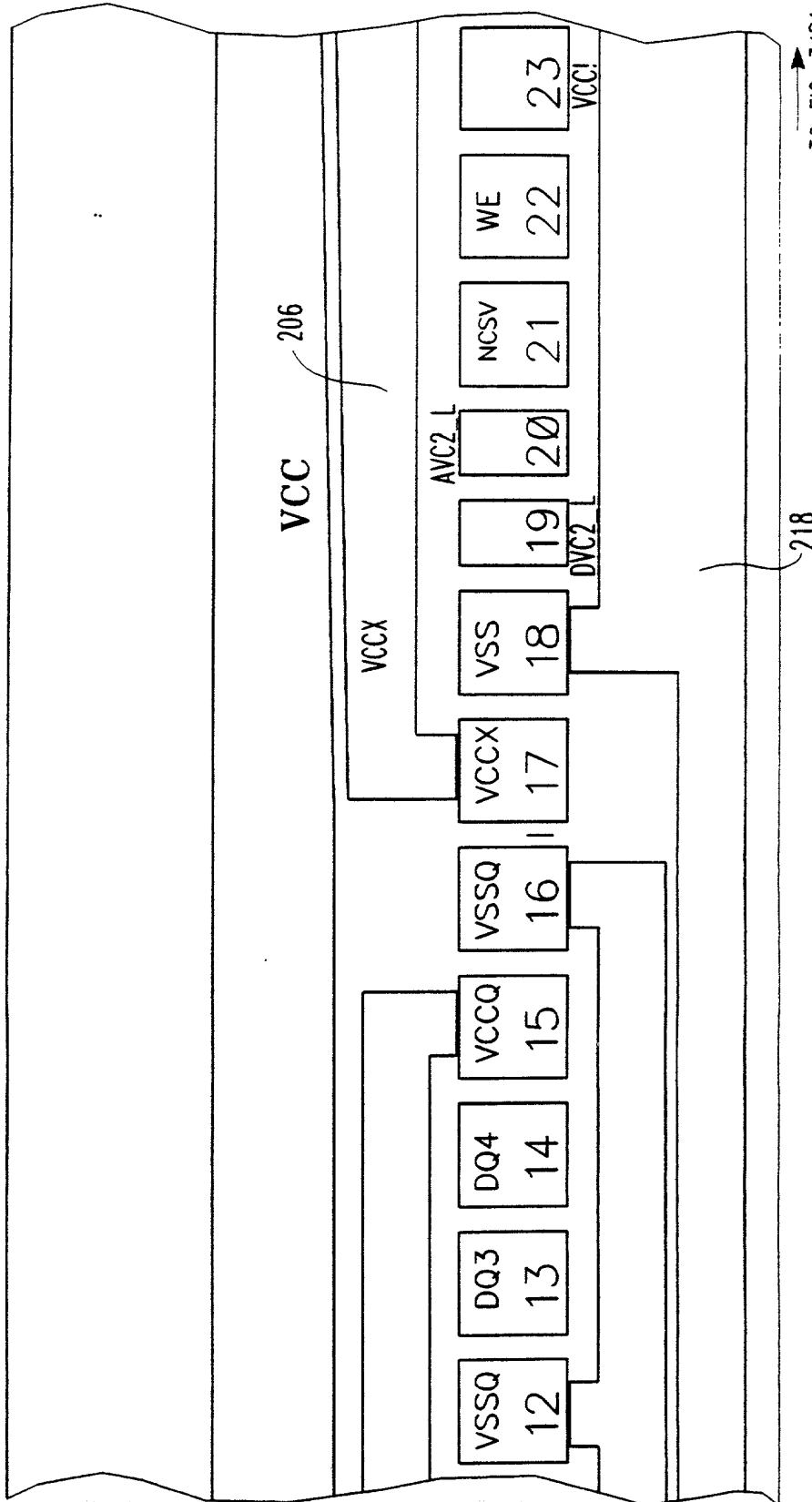
FIG. 33E4



TO FIG. 34A2

FIG. 34A1

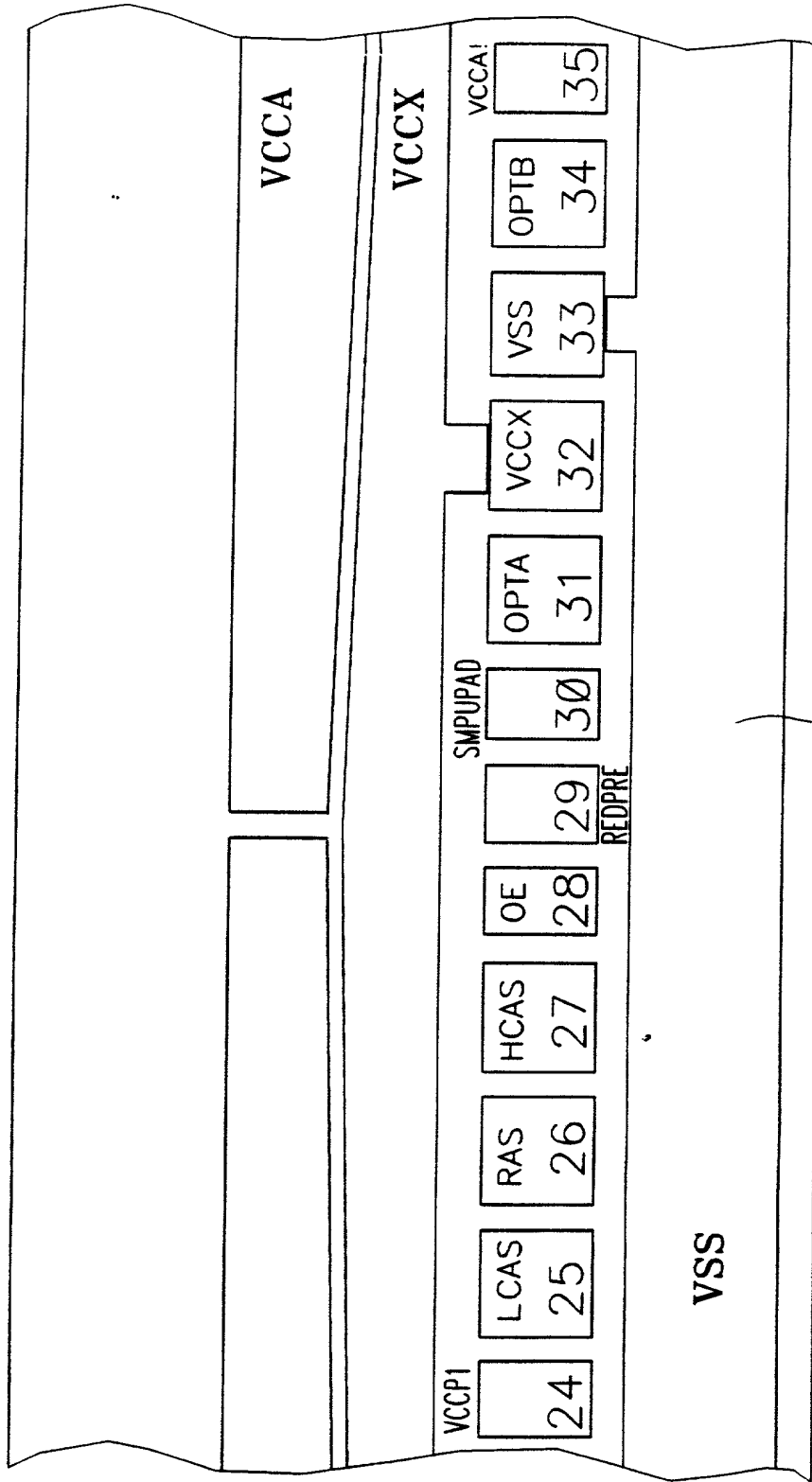
TO FIG. 34A1



TO FIG. 34B1

FIG. 34A2

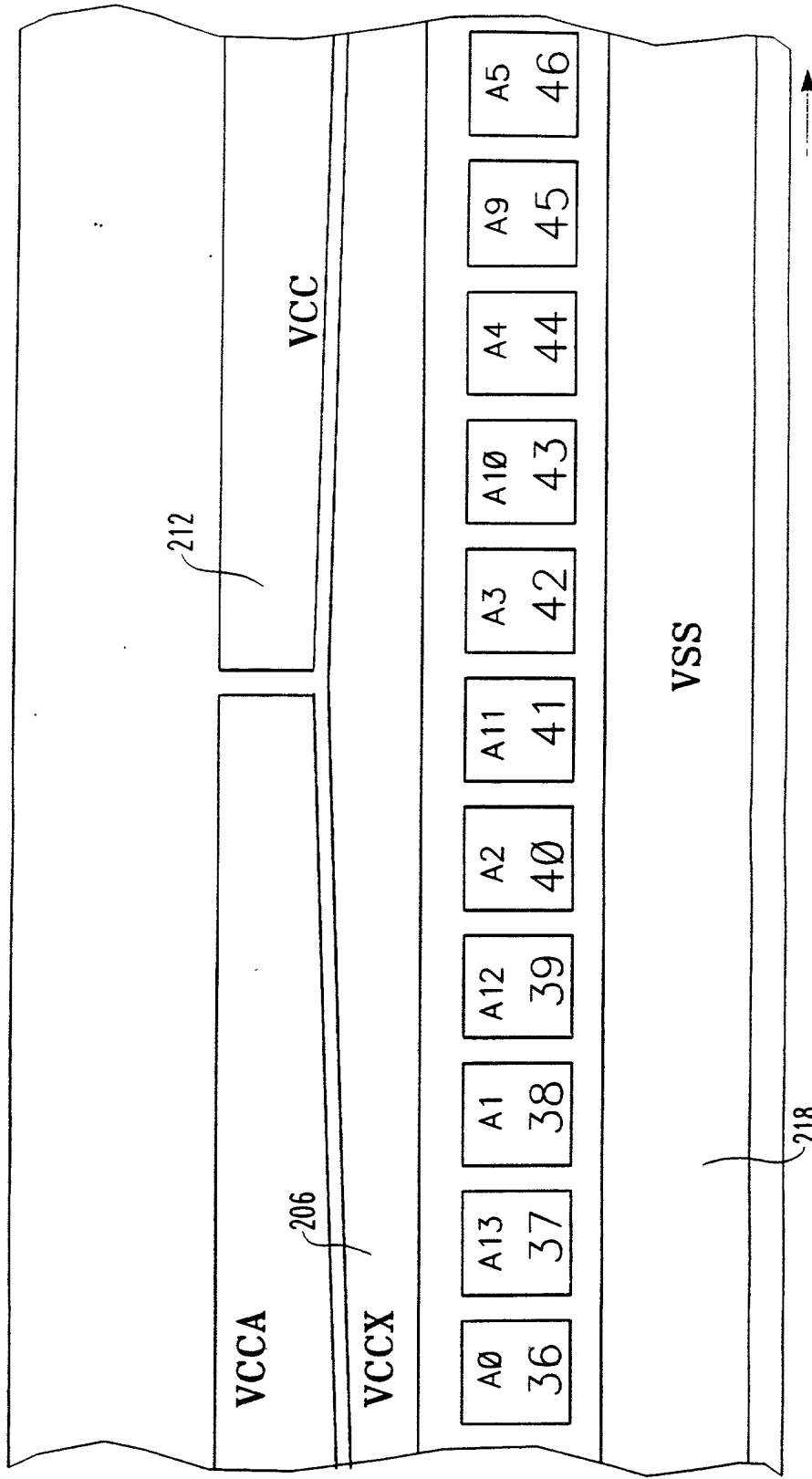
TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

TO FIG. 34B1

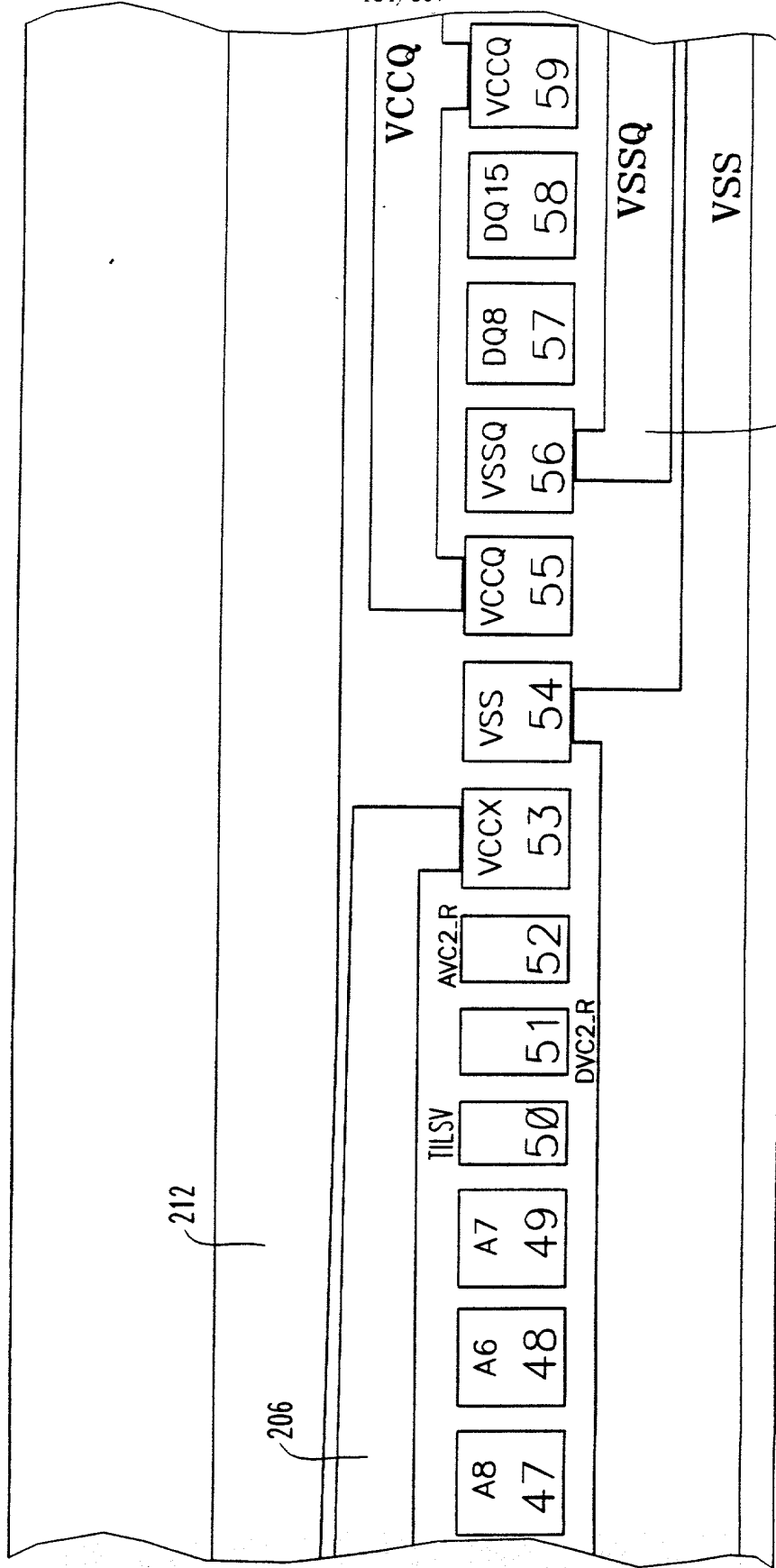


TO FIG. 34C1

FIG. 34B2

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TO FIG. 34B2



TO FIG. 34C2

FIG. 34C1

TO FIG. 34C1

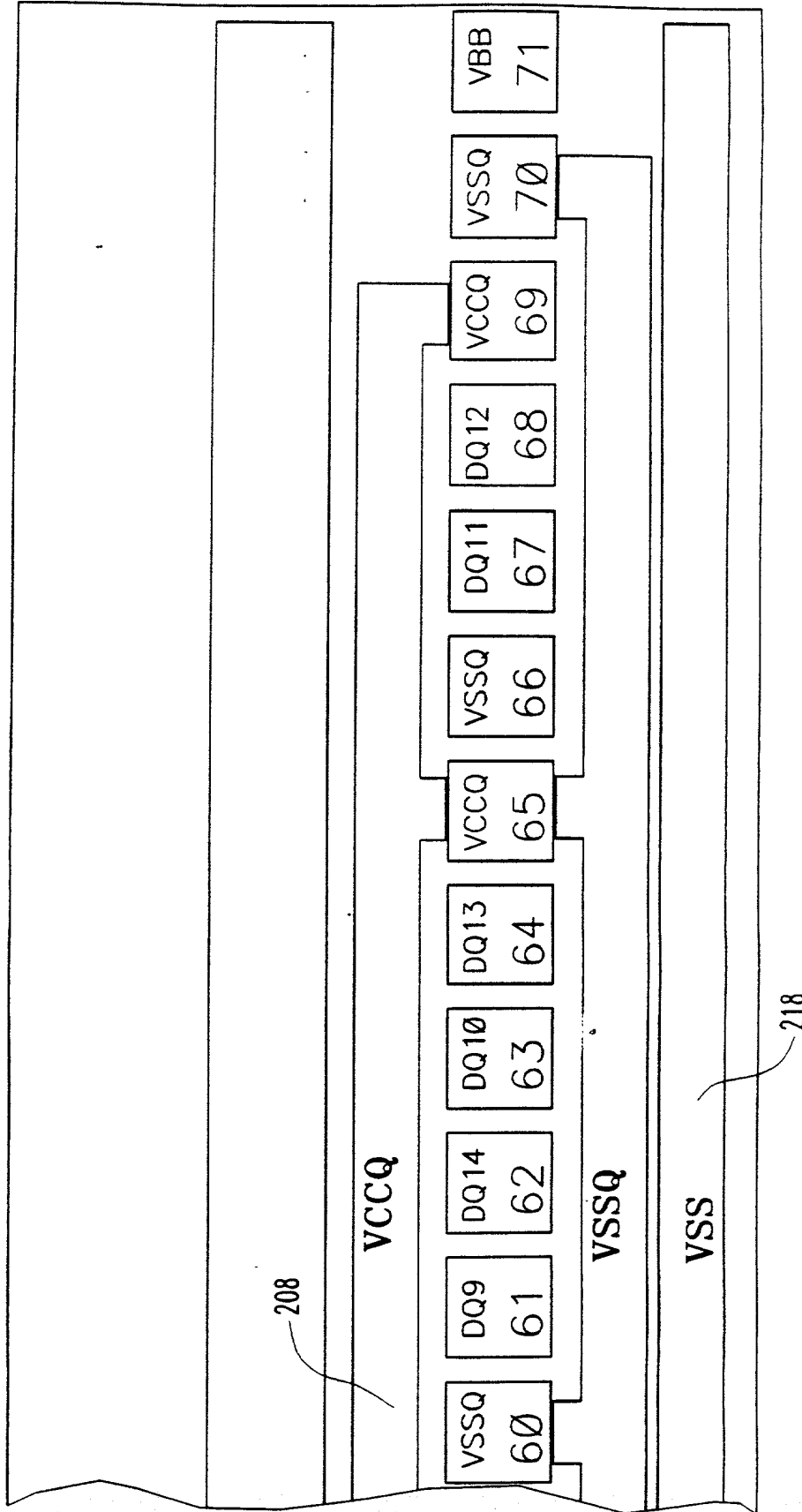


FIG. 34C2

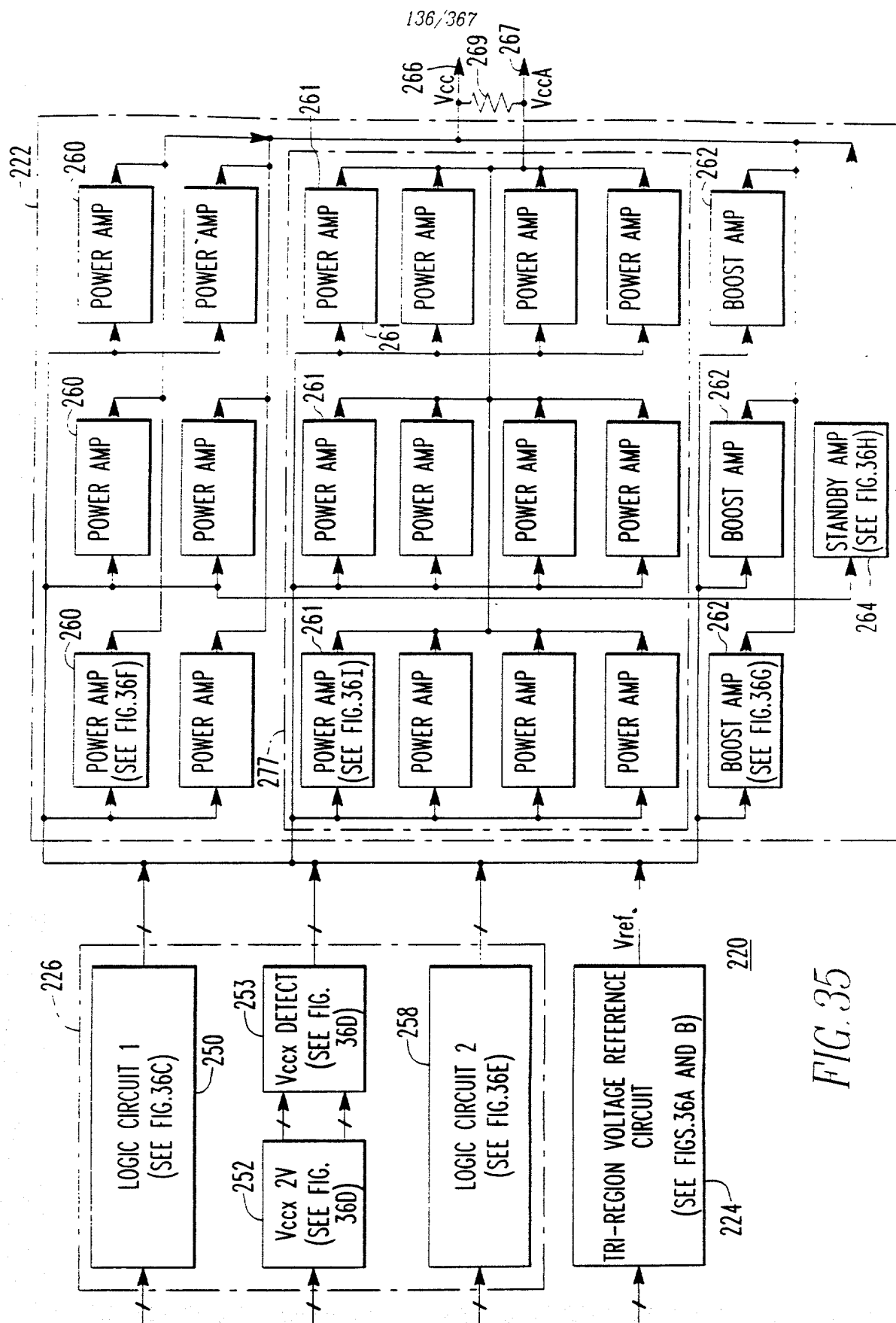


FIG. 35



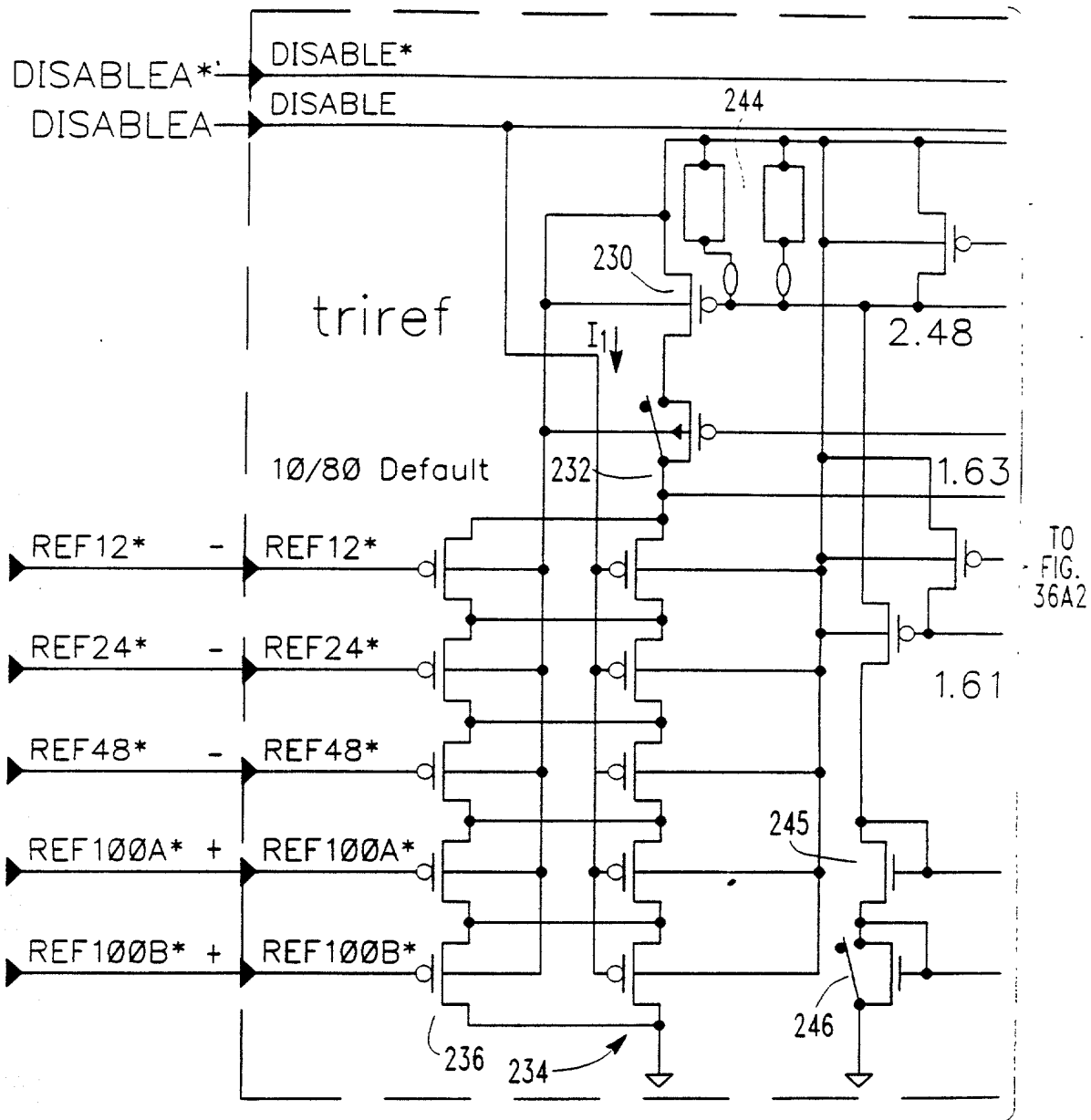


FIG. 36A1

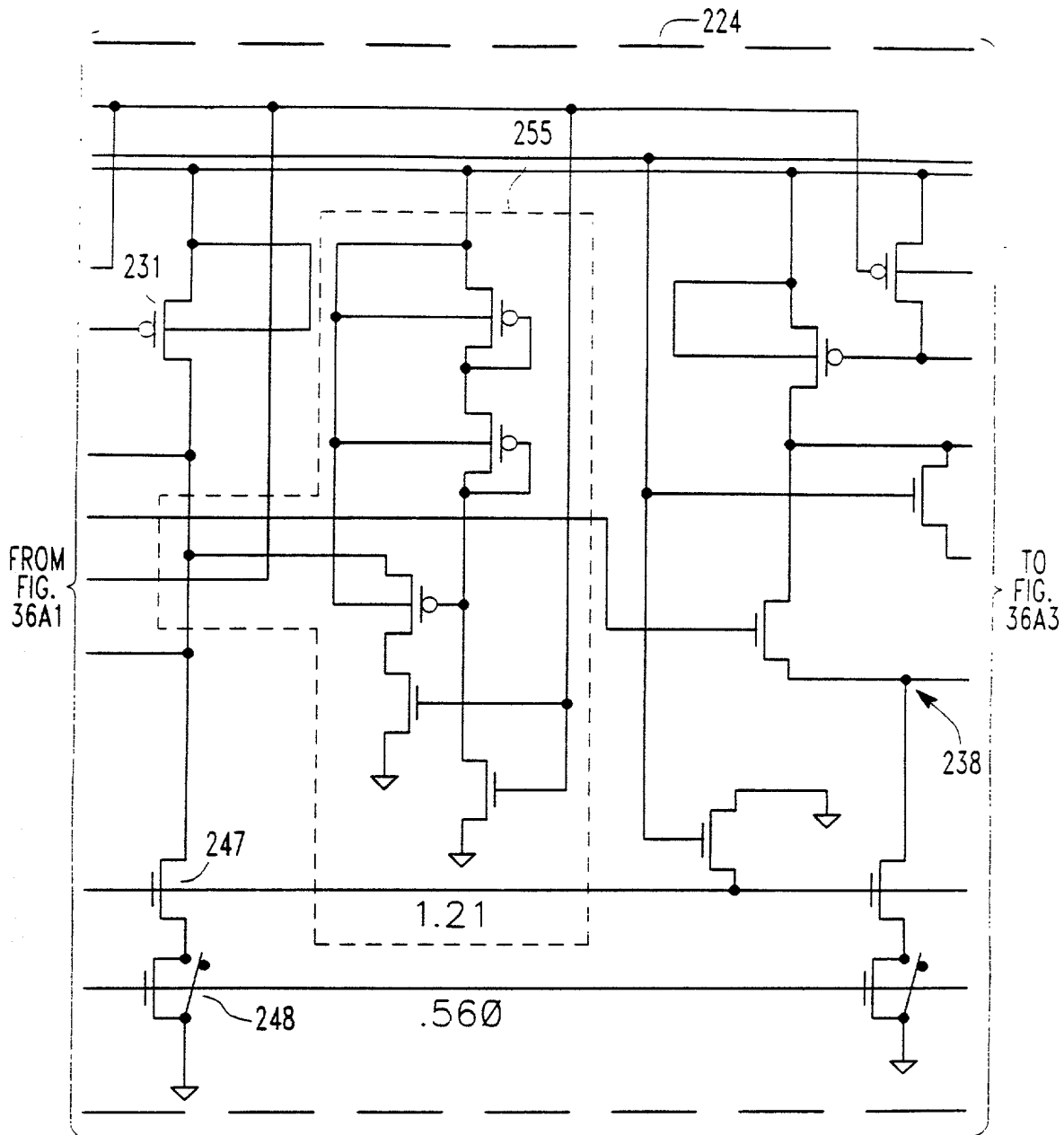


FIG. 36A2

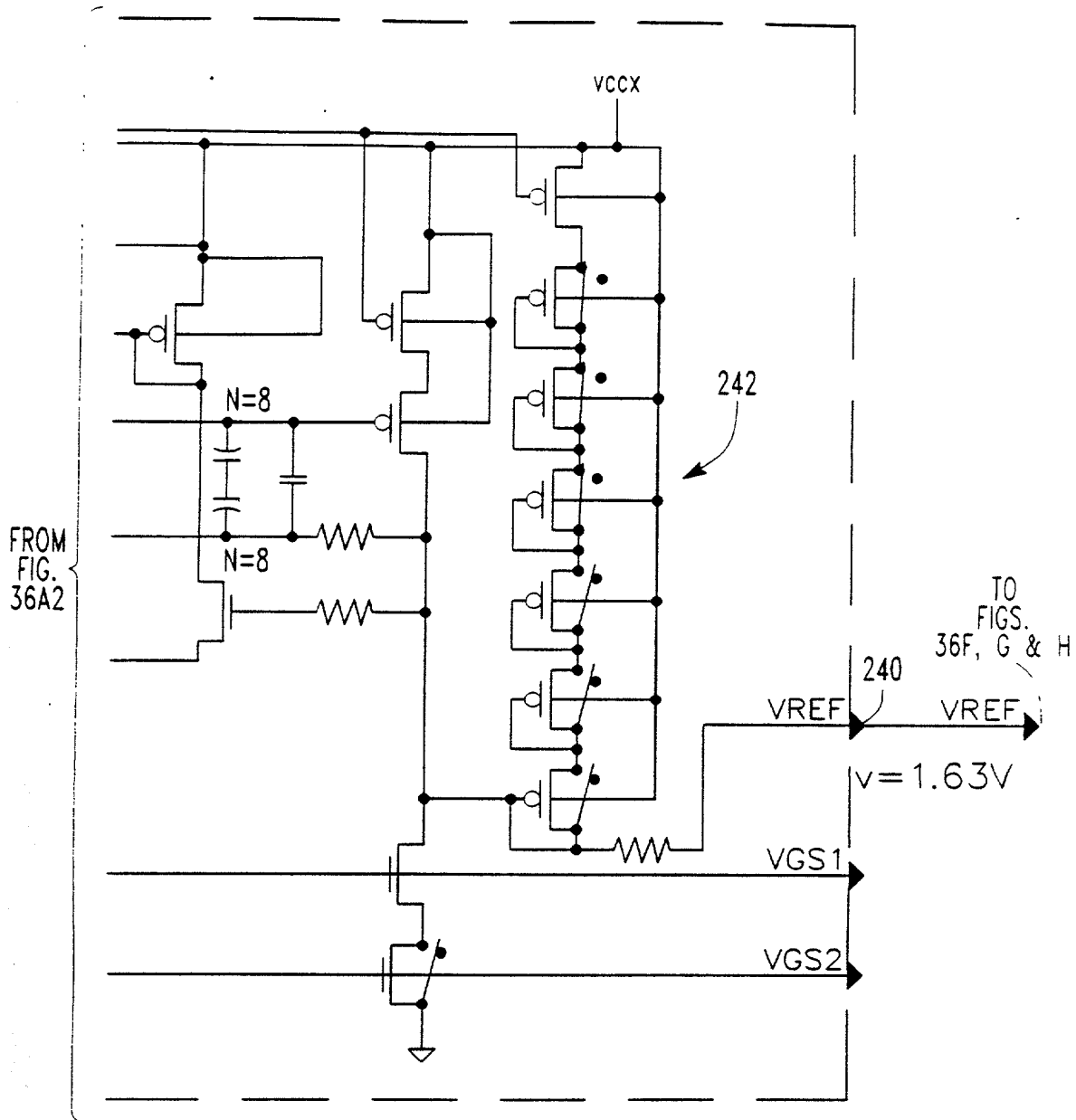


FIG. 36A3

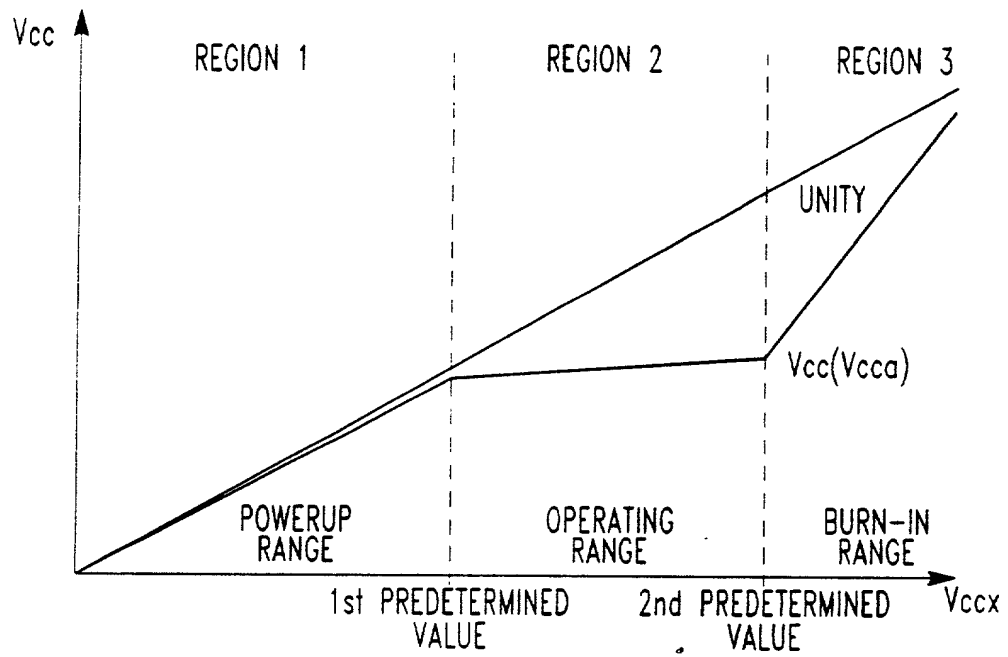


FIG. 36B

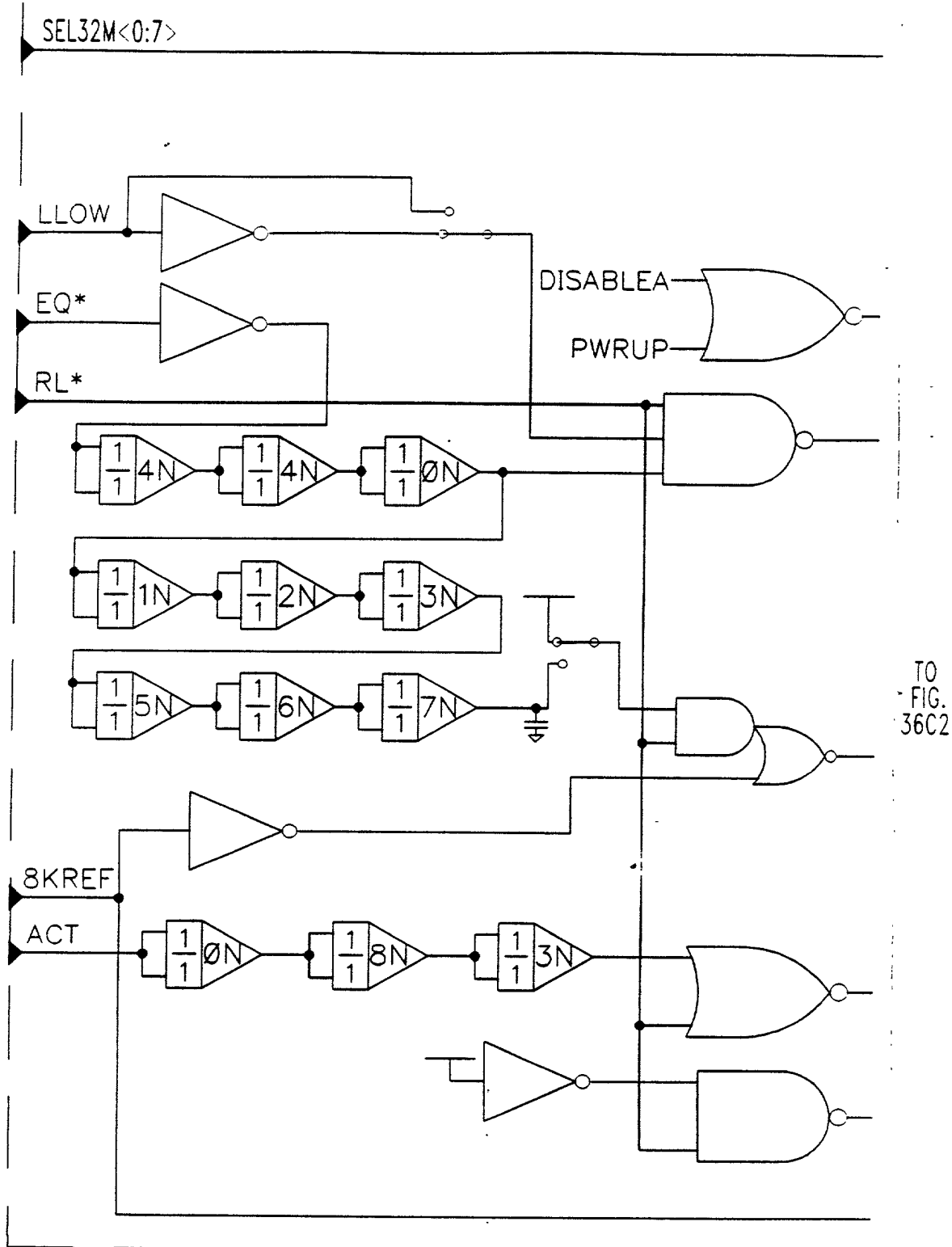
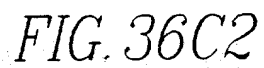


FIG. 36C1



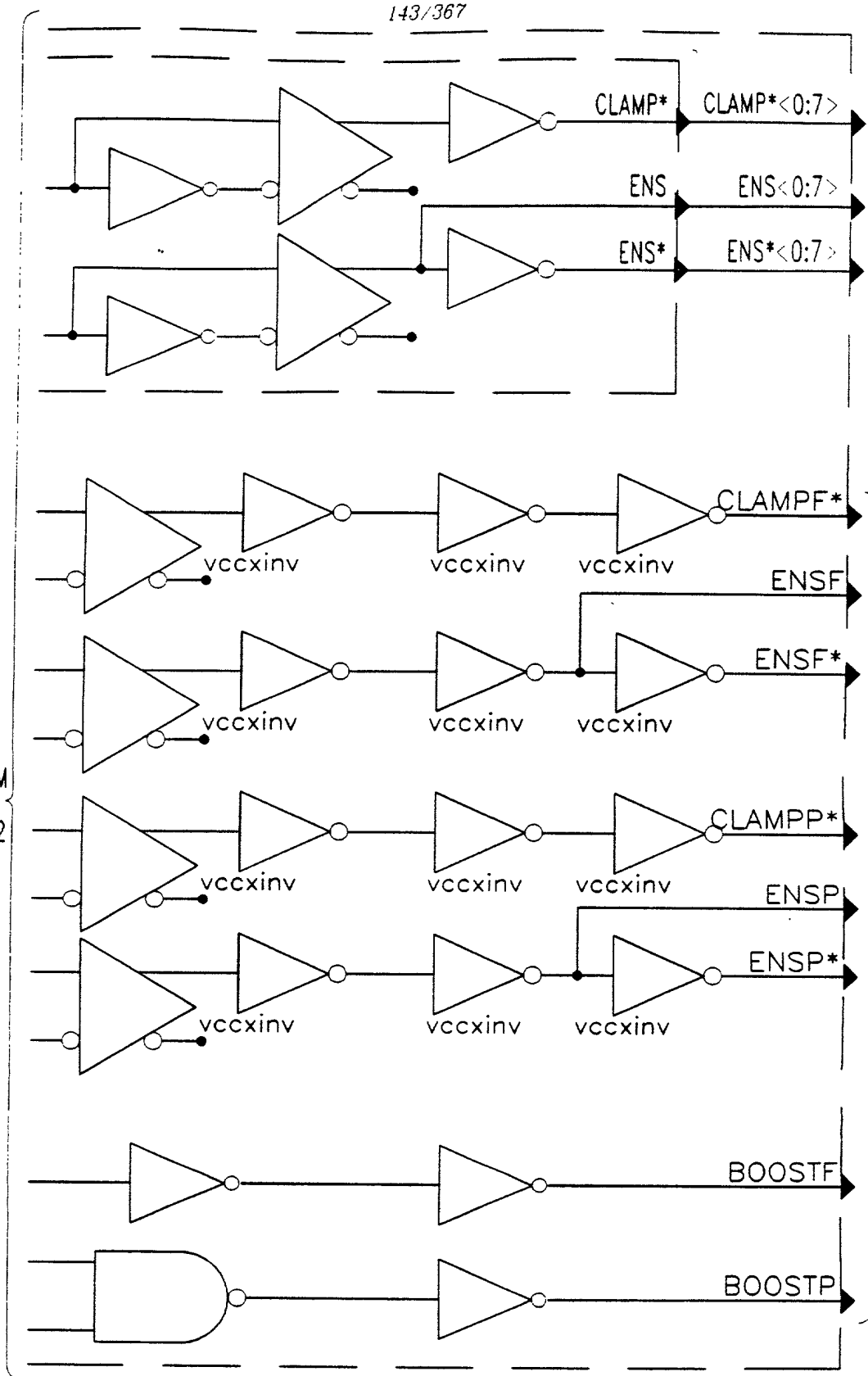
FROM  
FIG.  
36C2TO  
FIG.  
36F

FIG. 36C3

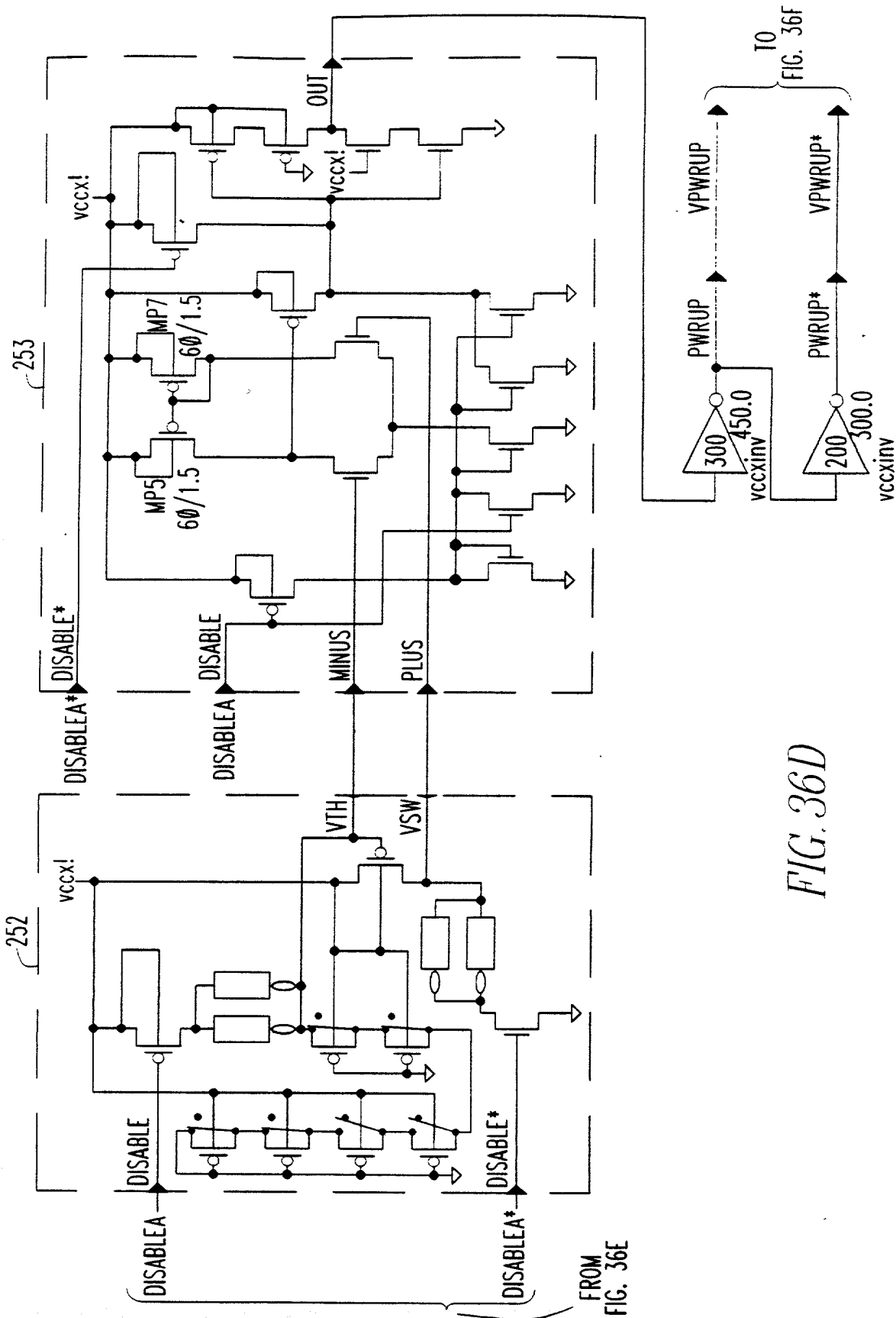
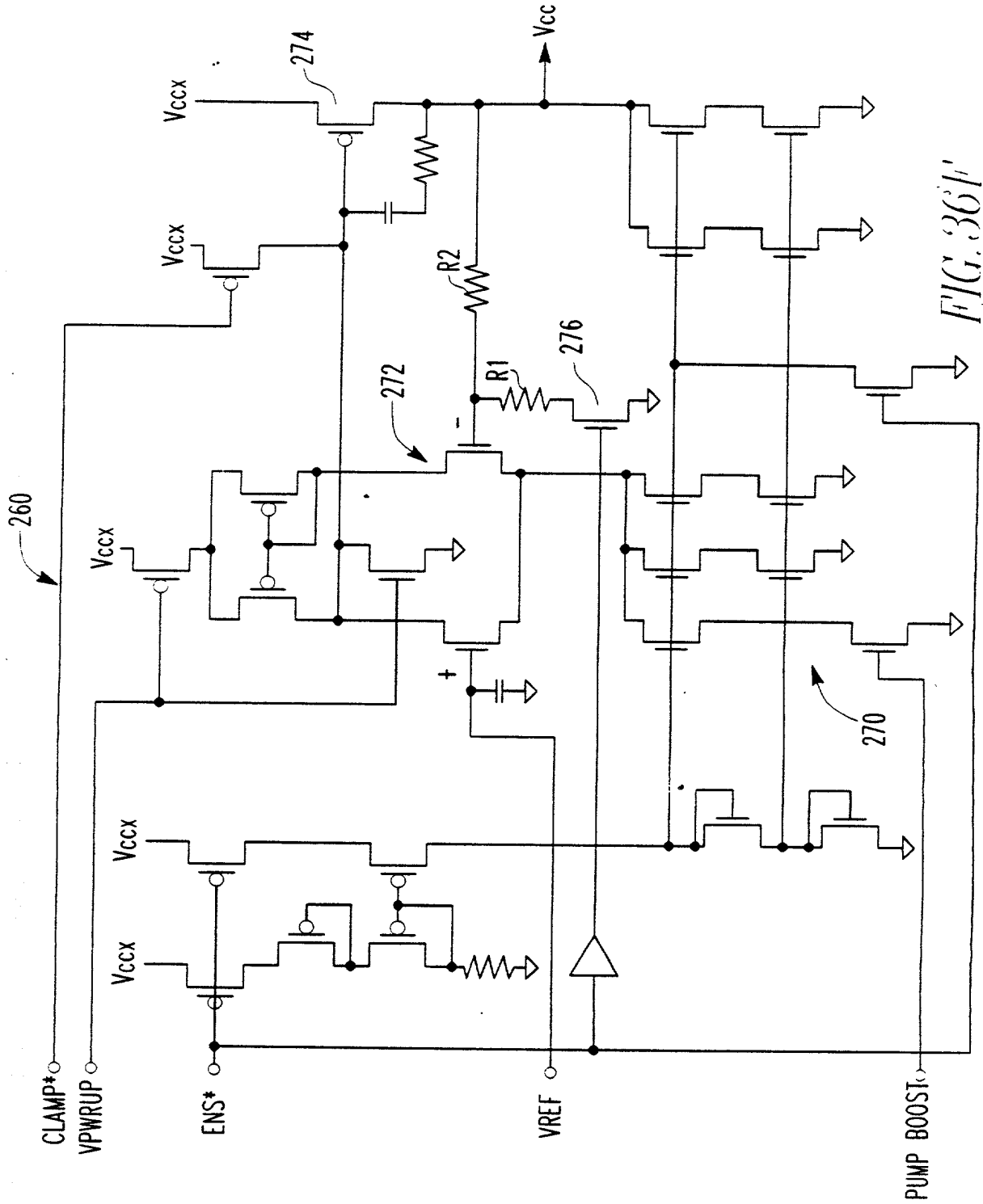
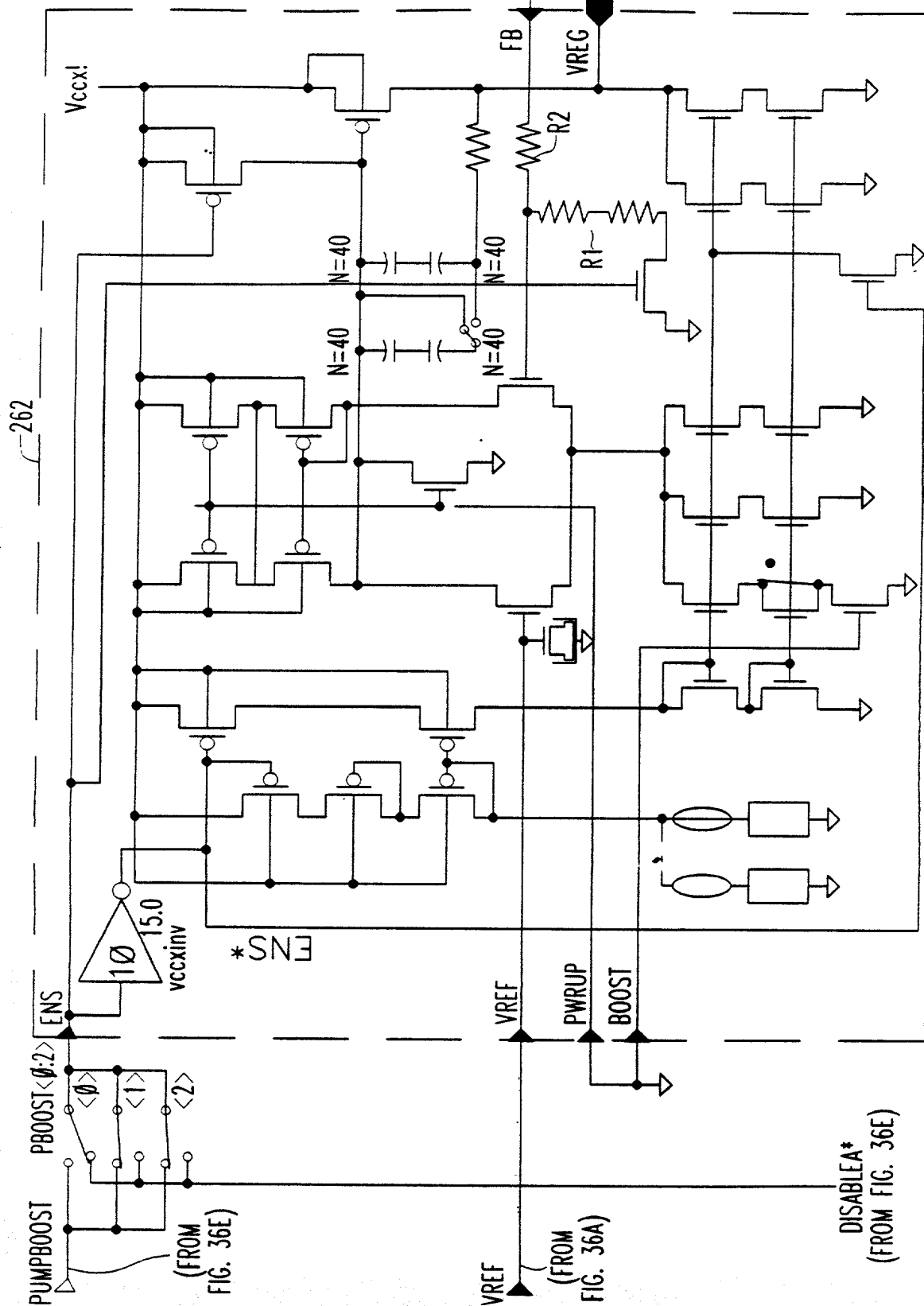


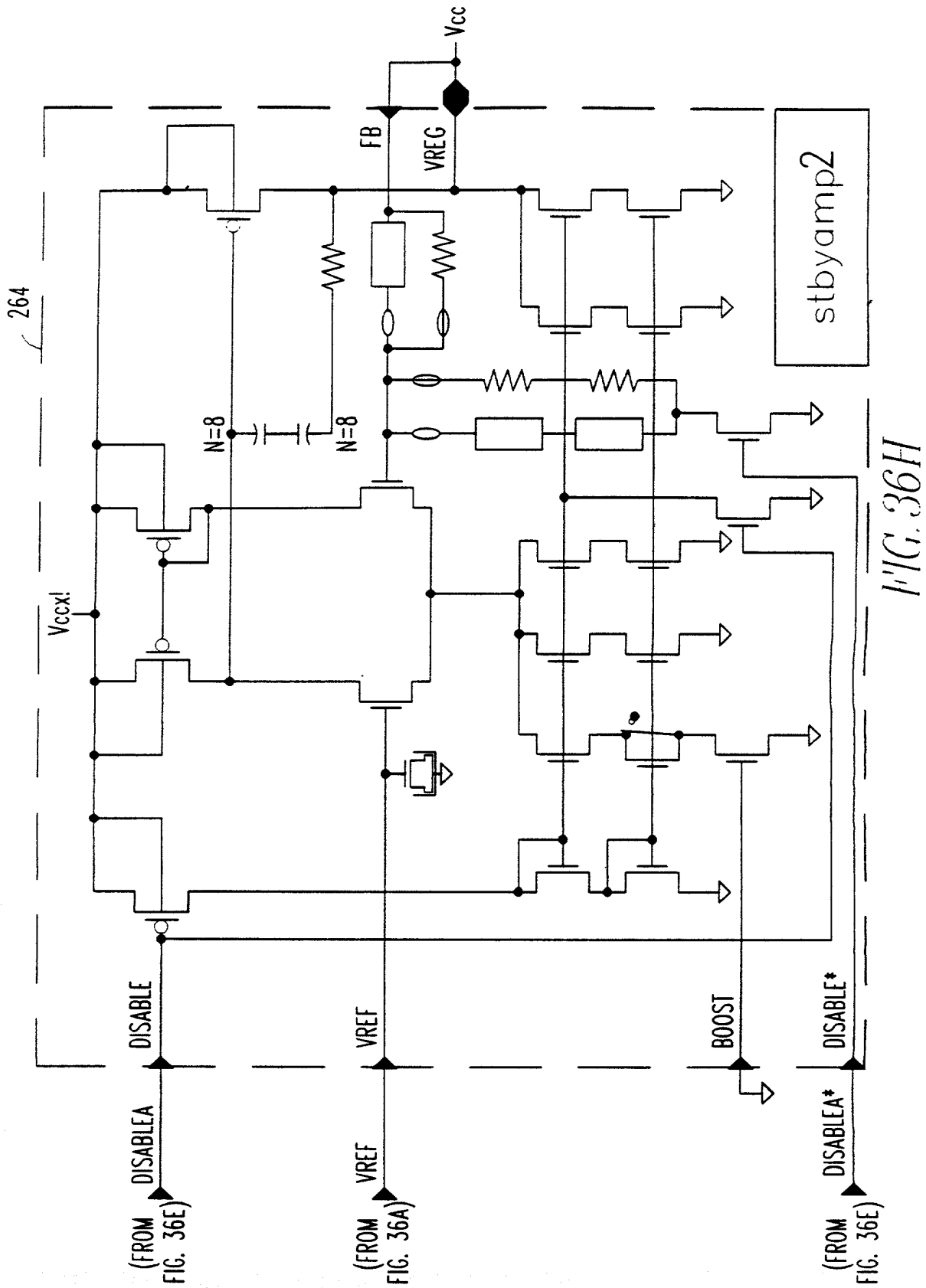
FIG. 36D

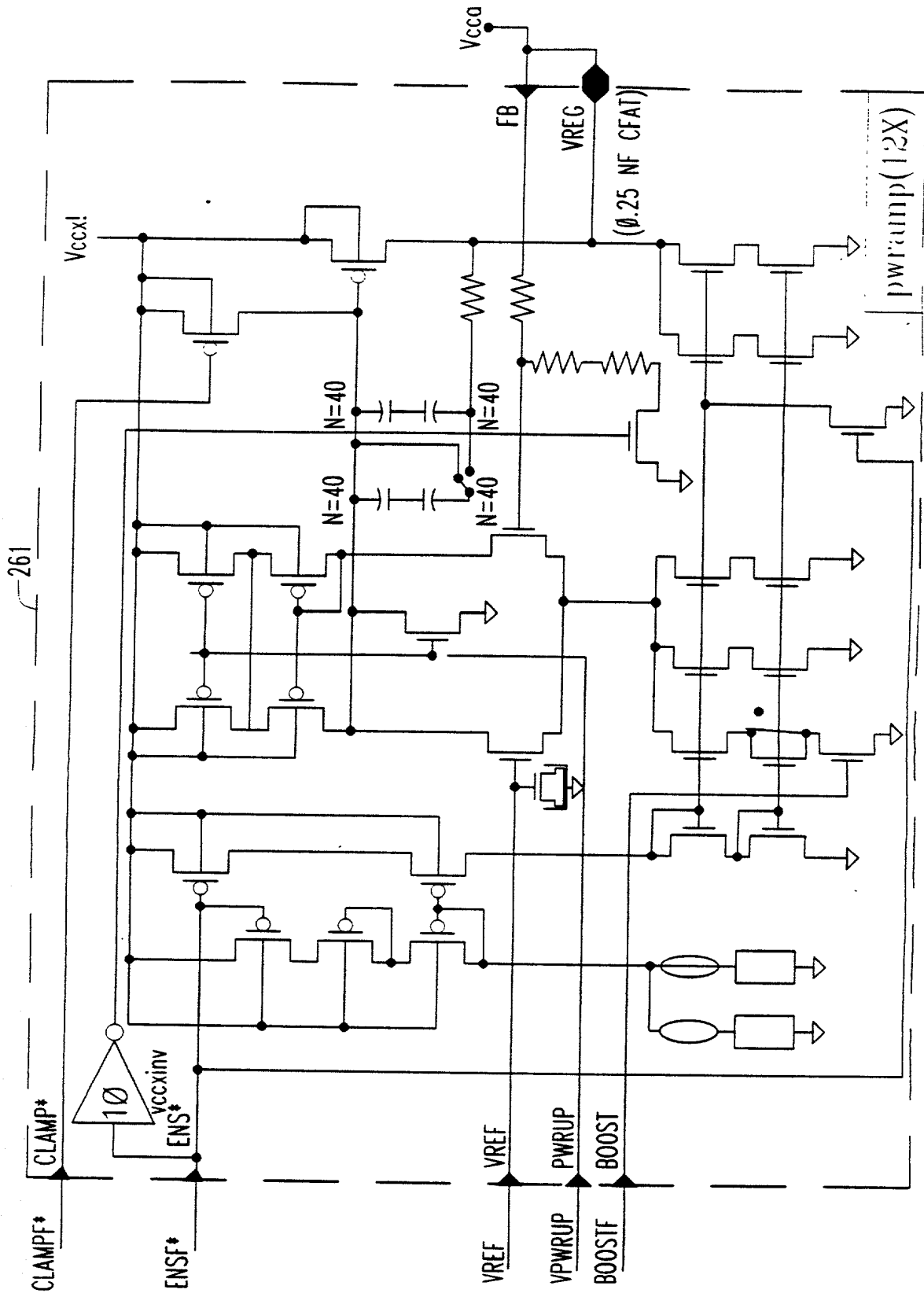












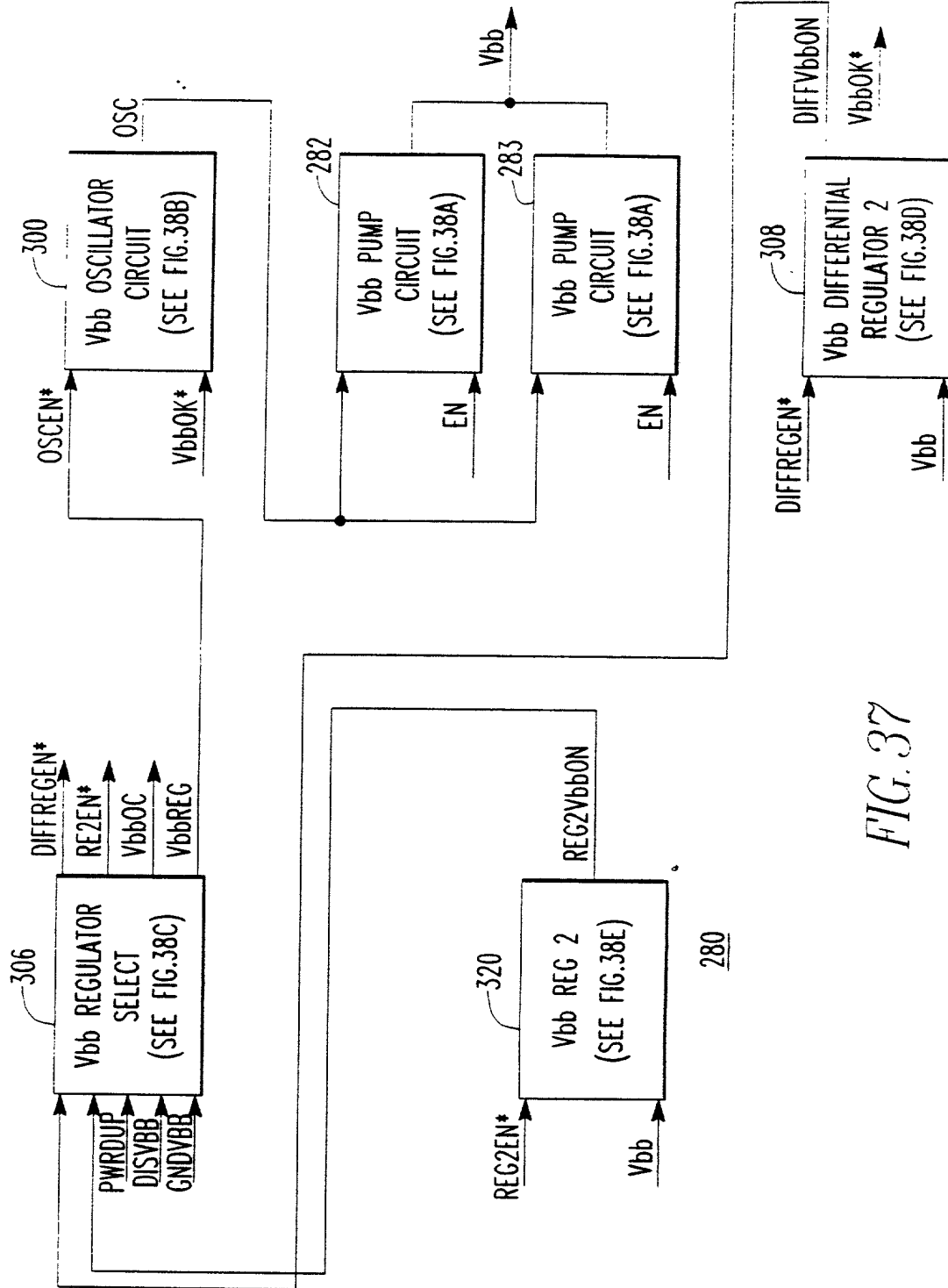
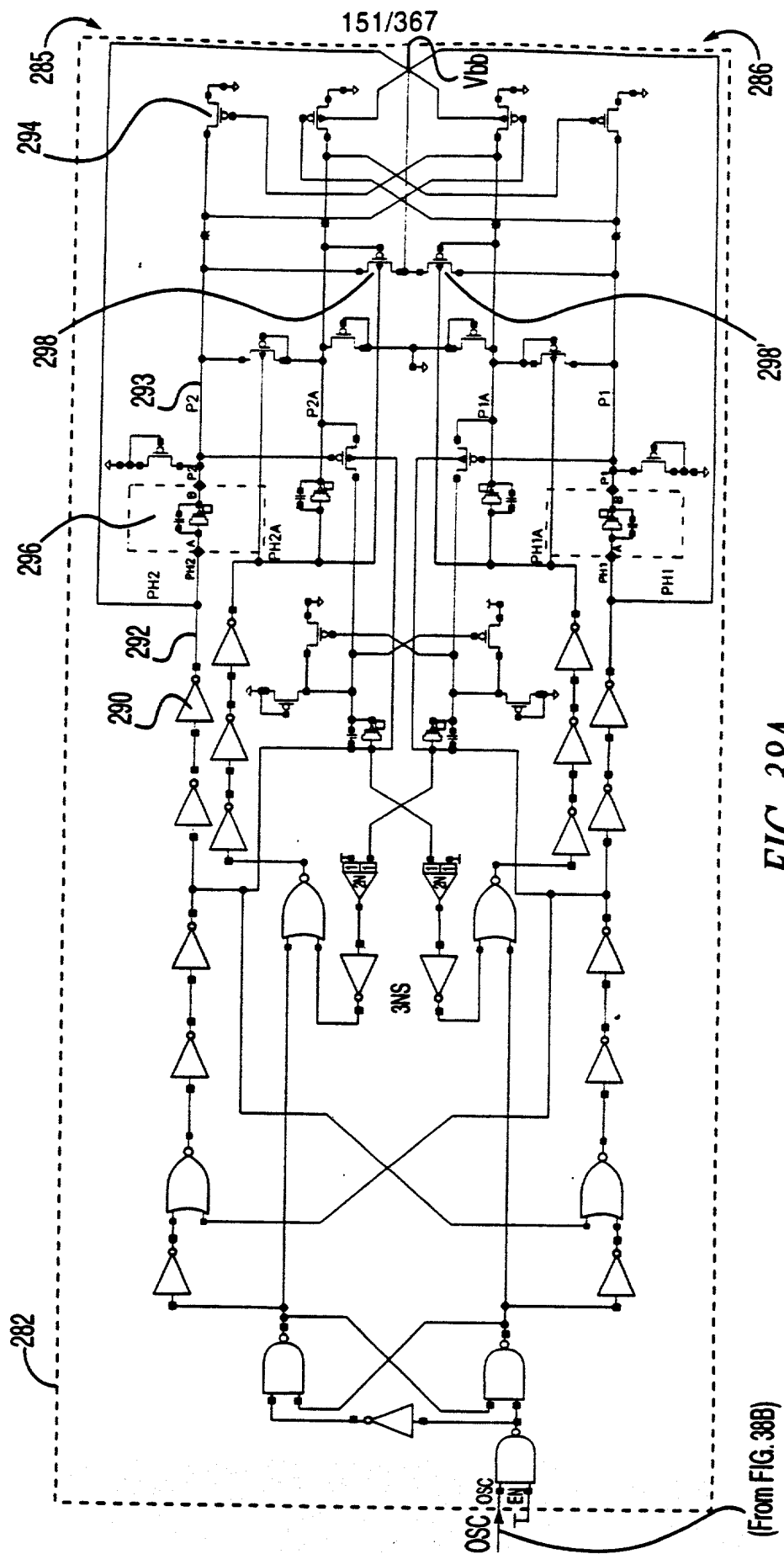


FIG. 37



(From FIG. 38B)